Technical University of Crete | SCHOOL OF ELECTRICAL & COMPUTER ENGINEERING

ECE Colloquium Spring 2021

16 Apr. 2021

Memristor-based *in-Memory* Logic Design Methodologies

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Universidad Técnica Federico Santa María
Valparaíso, Chile

Speaker

UNIVERSIDAD TECNICA FEDERICO SANTA MARIA

AC3E
Advanced Center for Electrical & Eleectronic Engineering

Short CV

Education

2010 to 2014 **Ph.D.** degree from the **Dept. of Electrical & Computer Eng.** of the **Democritus University of Thrace** (**DUTh**) in **Greece**

2003 to 2008 **M. Eng.** (**Diploma**) degree from the **Dept. of Electrical & Computer Eng**. of the **Democritus University of Thrace** (**DUTh**) in **Greece**

Recent Professional Experience

11/2018 to - **Adjunct Researcher** with the **Data Analytics & Artificial Intelligence Group** of the **Advanced Center of Electrical & Electronic Engineering** (**AC3E**) in Valparaíso, Chile.

08/2017 to - **Assistant Professor** with the **Dept. of Electronic Eng.** of the **Universidad Técnica Federico Santa María** (**UTFSM**) in Valparaíso, Chile

11/2015 to 07/2017 **Post-doctoral Researcher** with the **Dept. of Electrical Eng**. of the **Pontificia Universidad Católica de Chile (PUC)** in Santiago, Chile

Research Interests

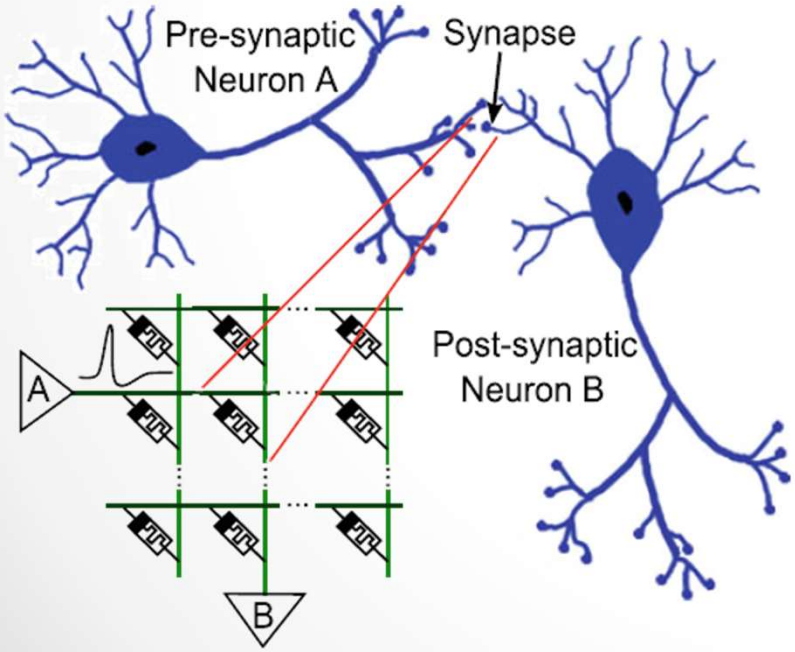
Resistive switching devices (memristors), unconventional & **neuromorphic computing**, software and HW aspects of **parallel computational** (bio-inspired) **circuits and systems**.

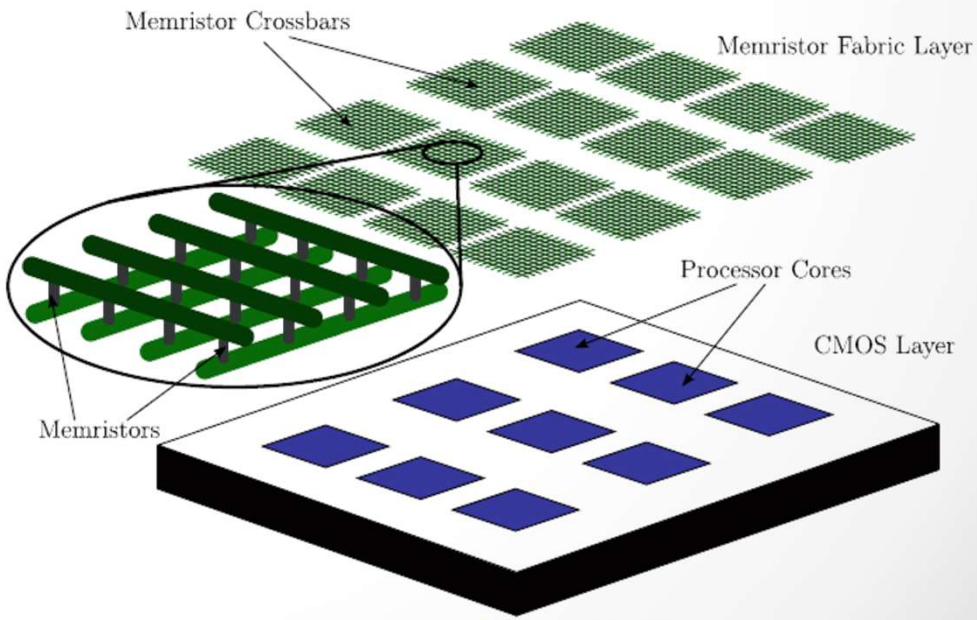
First stop in Chile…

Why?

CONICYT FONDECYT 3160042/2016

CLeArMeNu: "*Memristive Neural Computing & Learning Architectures*"





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FEDERICO SANTA MARIA

EX UMBRA IN SOLEM

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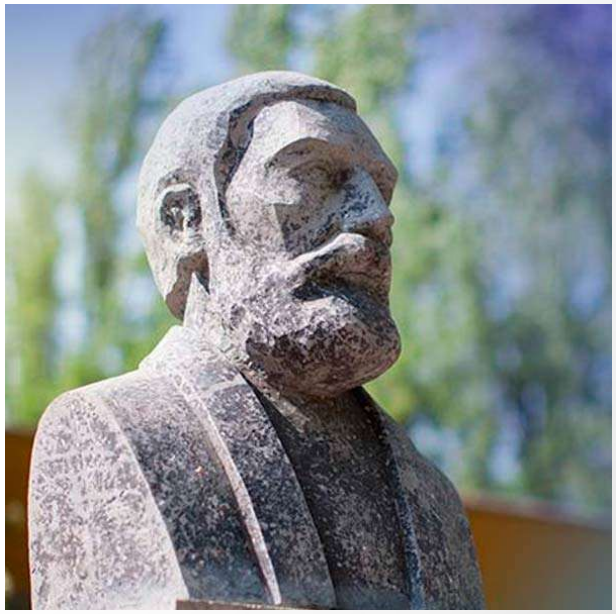

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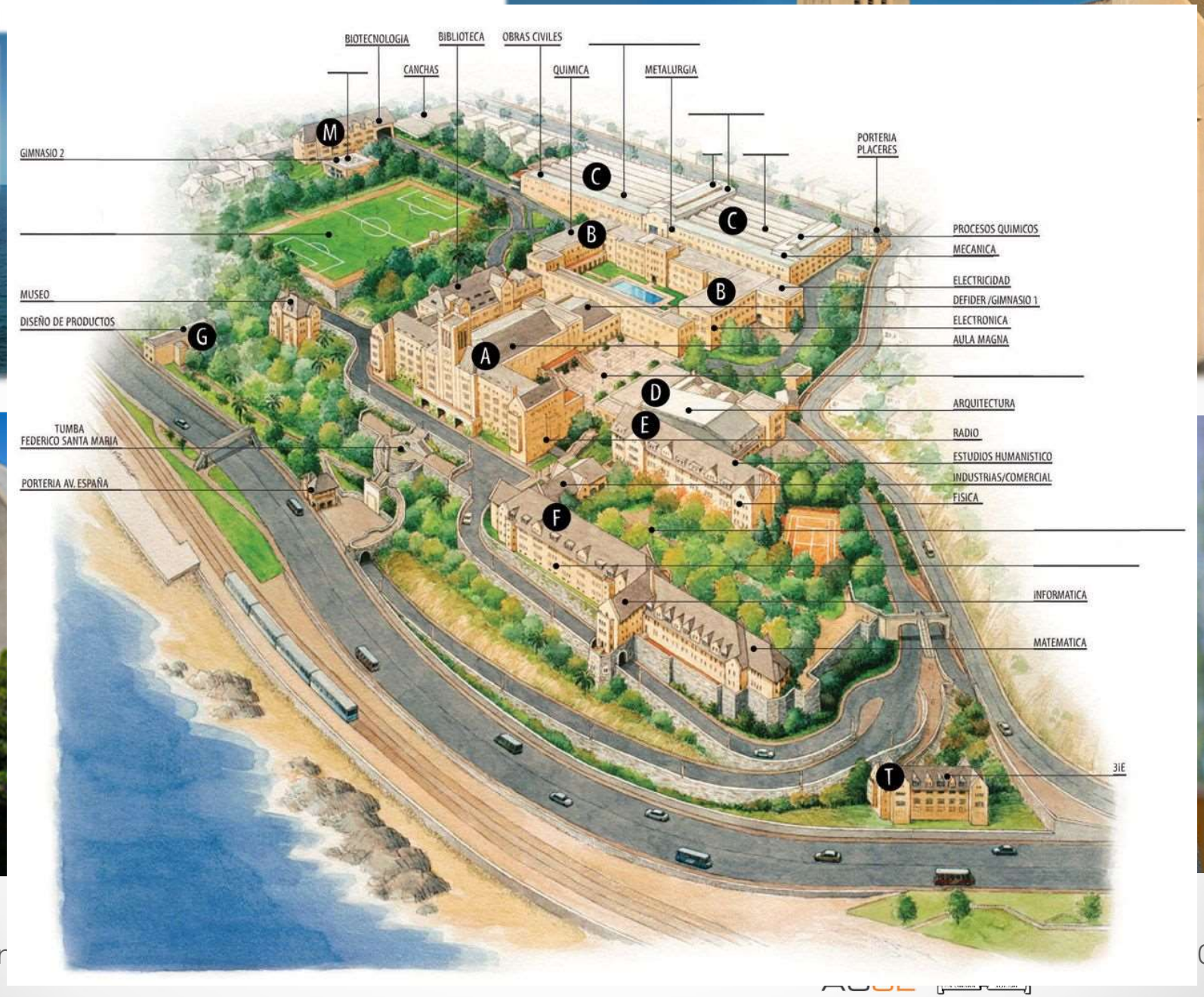


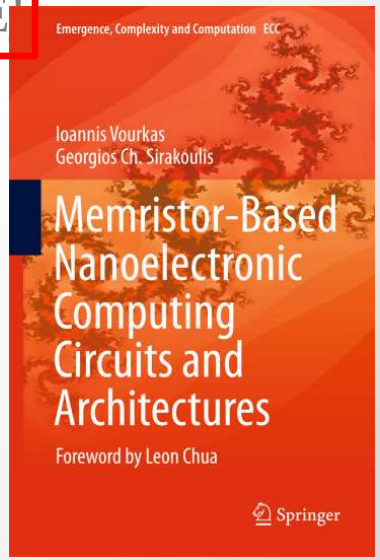
Research Work *Highlights*

Applications

Devices

- Memristive Networks as massively parallel comp. platforms
  IEEE TETC, WoS PPL
- Memristive Syncronization of complex nonlinear dynamical systems IEEE TCAS I, ELSEVIER Chaos, Solitons & Fractals
- Memristive ANNs for neuromorphic computing
  IEEE TNNLS
- Memristive multi-level resistive memory
  IEEE TVLSI, pending publications
- Memristive logic gates for *in-memory* computing
  IEEE TCAS II, TNANO, ELSEVIER MEL
- Memristor SPICE-level modelling
  IJCTA, IEEE TNANO, ELSEVIER SSE
- Memristor device characterization
  IEEE Access

…what this talk is about



Outline

Introduction to memristors

- The memristor as the forth fundamental circuit element
- Device types & most important properties
- Modeling of memristors

Memristor-based logic

- Motivation for in-memory logic with memristors
- Logic styles based on conditional switching of memristors
- Details of ratioed logic style robust to device variability

Experimental work with commercial memristors

- Related industry examples
- Ad-hoc instrumentation tools and basic circuit topologies
- Examples of measured device behavior
- Opportunities for collaboration

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The Memristor *in brief*

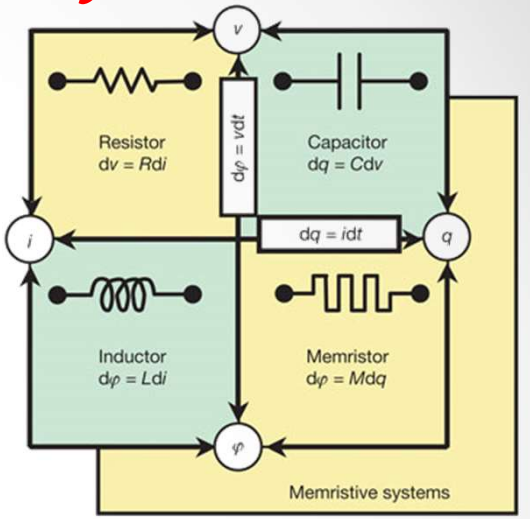
MEMory ResISTOR – MEMRISTOR

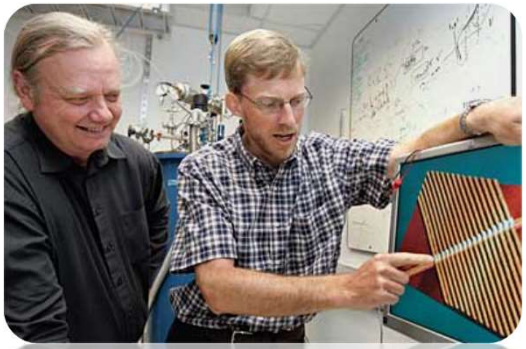
- Originally postulated by Leon Chua in 1971

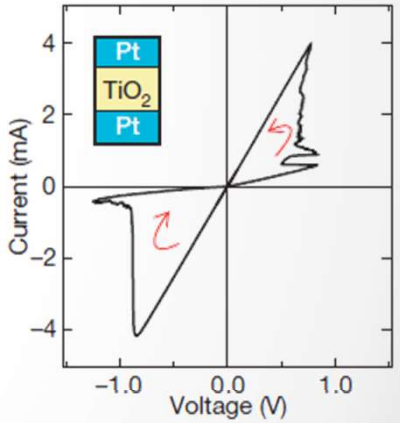
- Ever since the presentation of the "TiO_2" memristor and its connection with Chua's theory made by HP Labs in 2008 (the first RS devices were known from the 60s), it has drawn great attention by both academia and industry

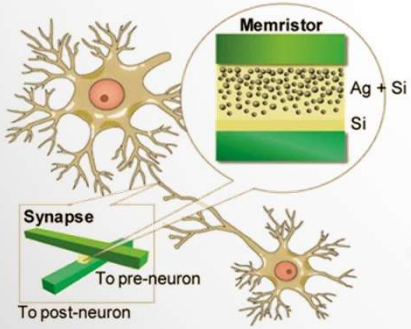
- **To date**, memristor represents a technology breakthrough which creates new opportunities for realization of innovative circuits

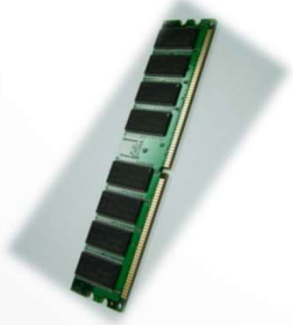
- **Applications**: Non-volatile memory, adaptive circuits, signal processing, Logic/computing, …

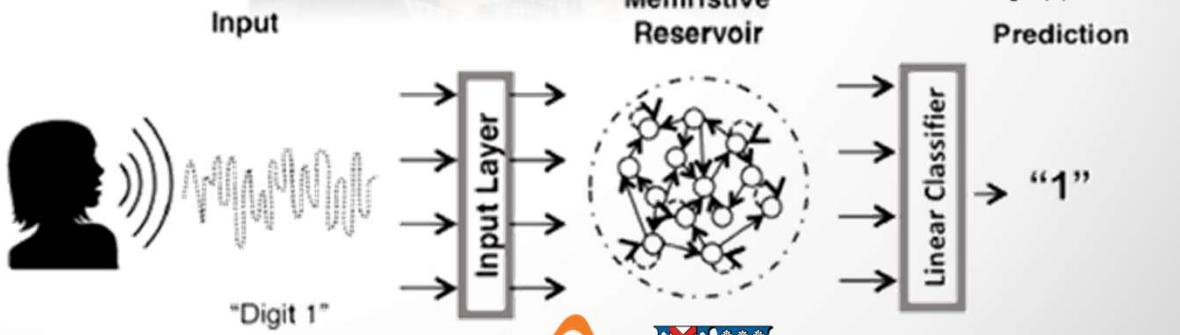












The 4th Element

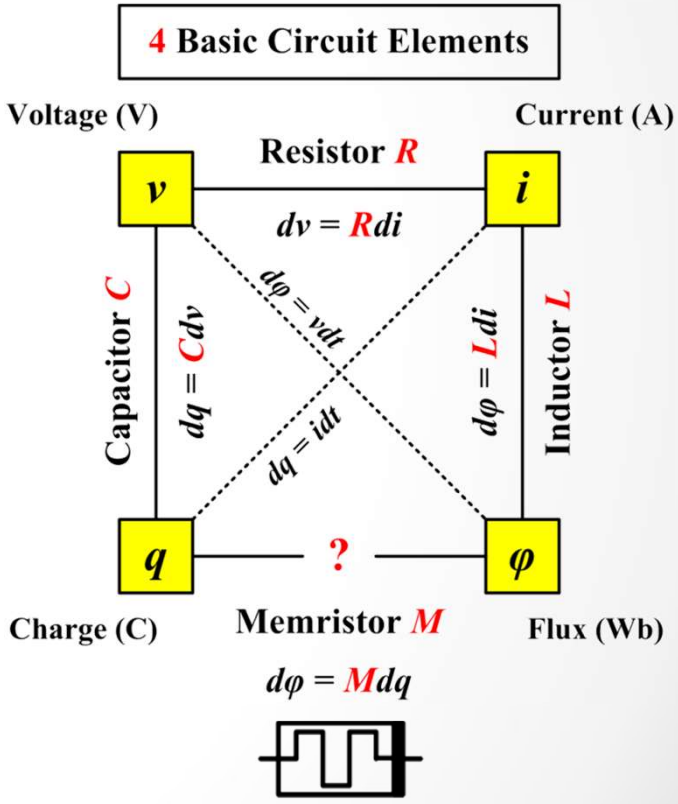
The **ideal memristor** was first introduced as a 2-terminal circuit element that linked the remaining pair of the four basic circuit variables

Later in 1976 it was generalized to the class of **memristive devices**

Defined via a **state-dependent Ohm's Law :**

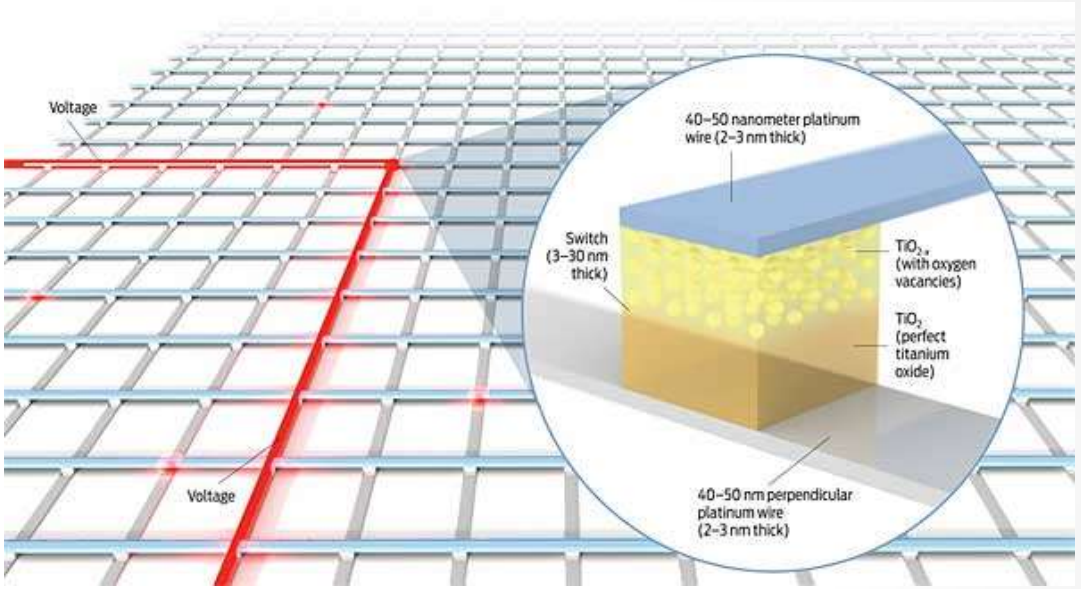
Current-controlled Memristor	Voltage-controlled Memristor
$v = R(x)i$	$i = G(x)v$
$\frac{dx}{dt} = f(x,i)$	$\frac{dx}{dt} = g(x,v)$

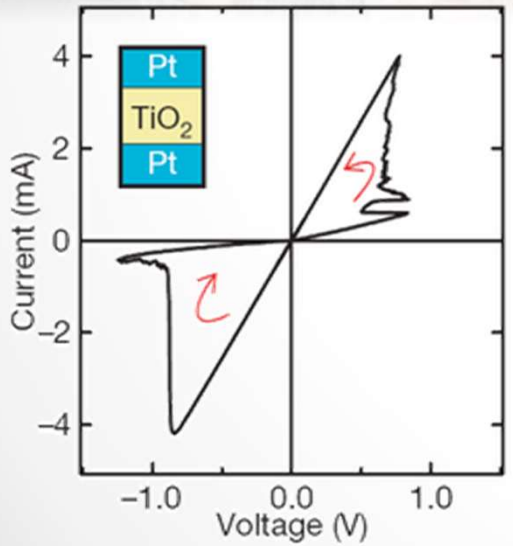
State-vector $\boldsymbol{x} = (x_1, x_2, \ldots, x_n)$ has $n \geq 1$ components $x_1, x_2, \ldots x_n$ called *state-variables,* which represent internal physical parameters of a specific device

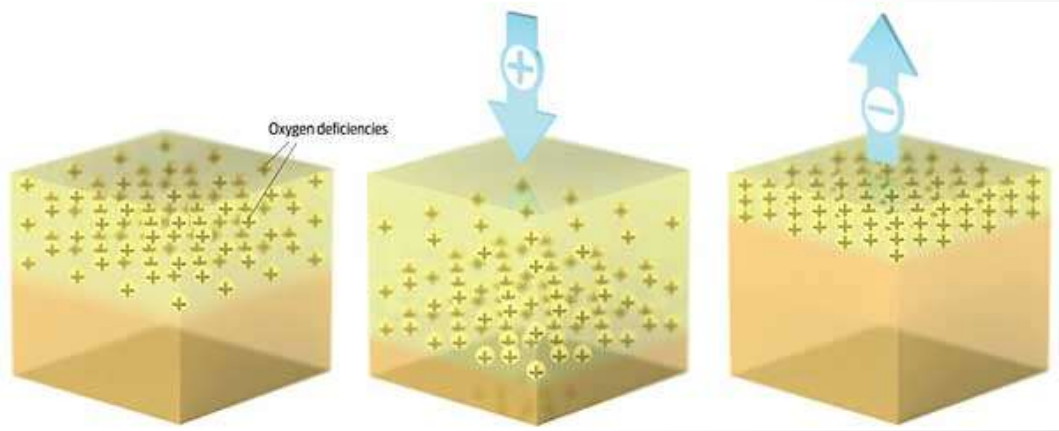


The *missing* Memristor Found!

D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "**The missing memristor found**," *Nature*, vol. 453, pp. 80-83, 2008



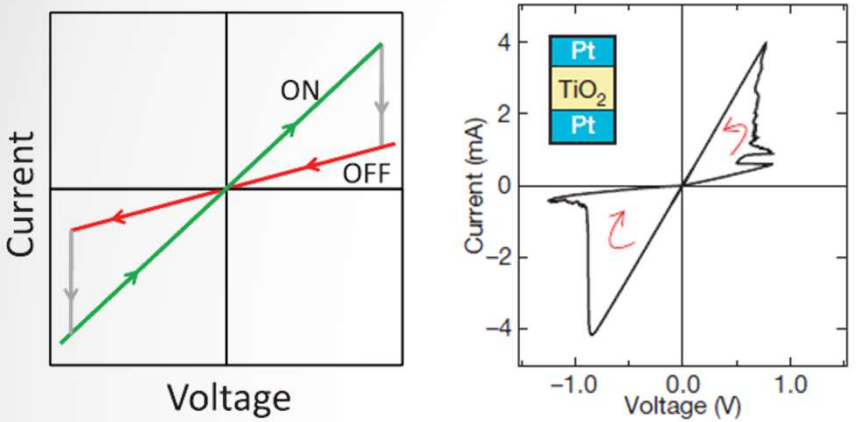




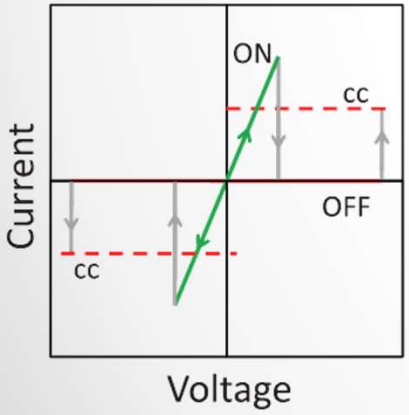
Memristor *Device Types* & *Properties*

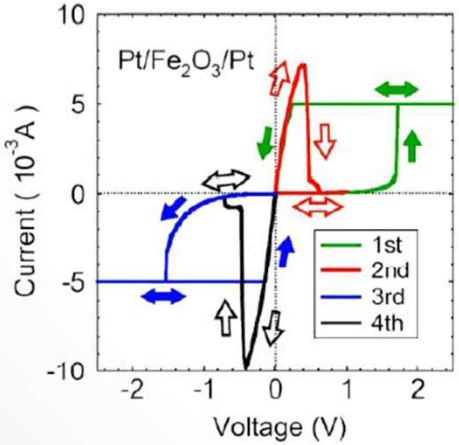
Commonly observed *i-v* types

Bipolar



Unipolar





G. Sassine *et al.*, "Interfacial versus filamentary resistive switching in TiO2 and HfO2 devices," *J. Vac. Sci. Technol*. vol. B34 (012202), 2016

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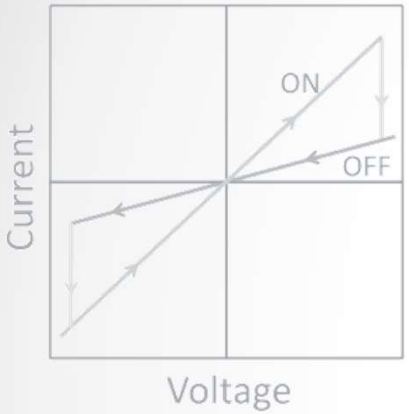
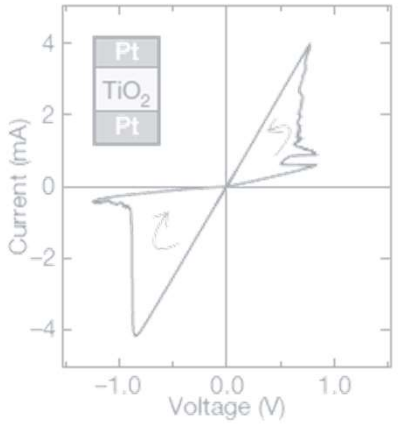
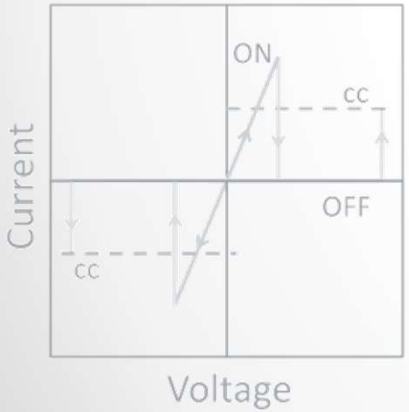
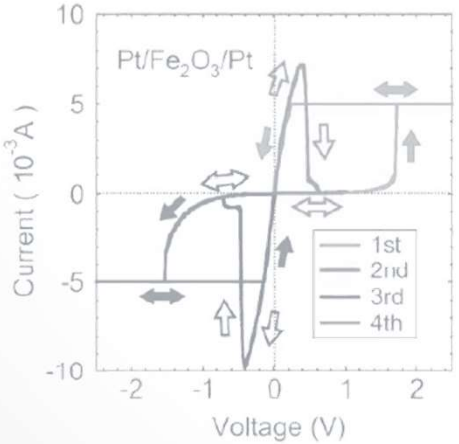
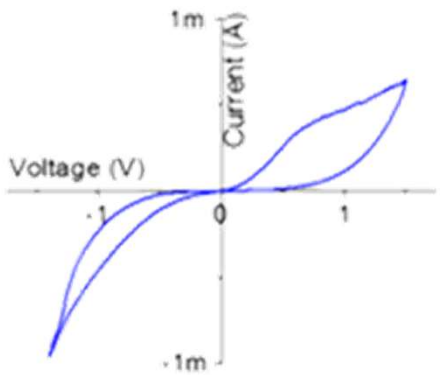


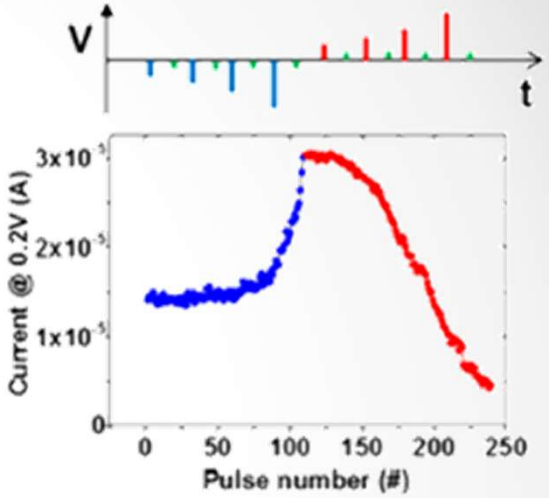


Unipolar

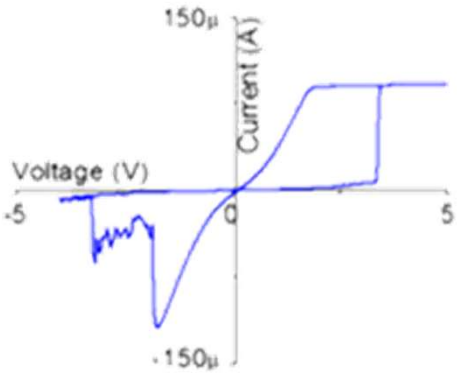


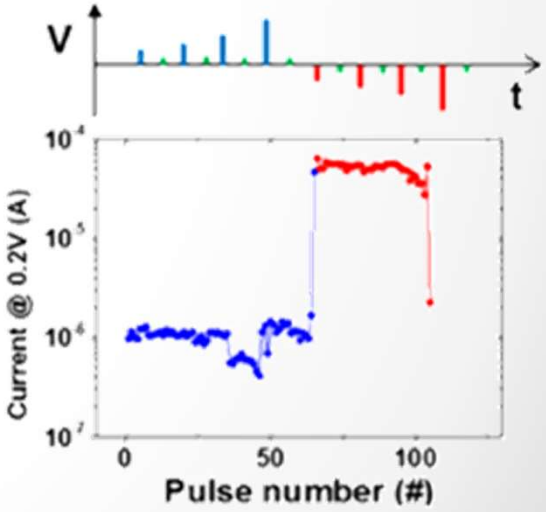






Interfacial (analog)



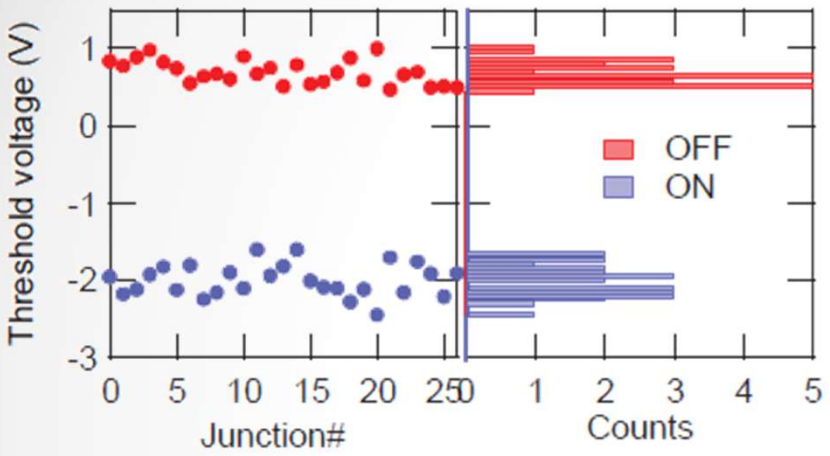


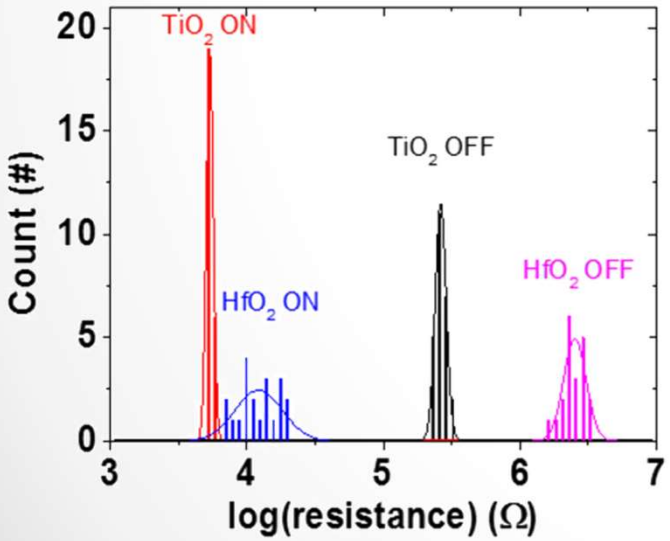
Filamentary (binary)

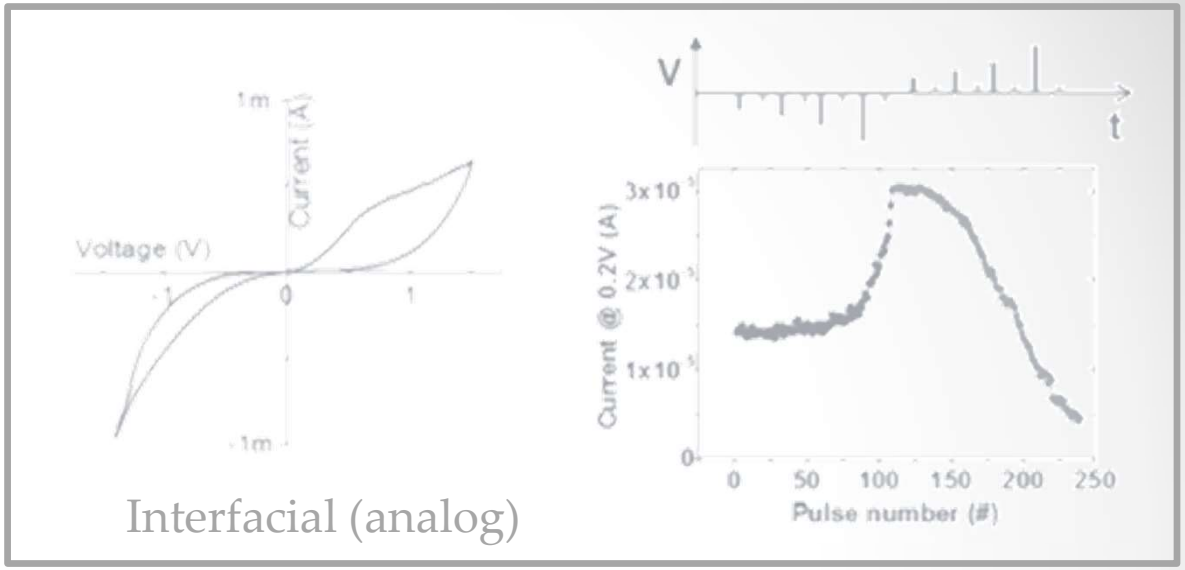
G. Sassine *et al.*, "Interfacial versus filamentary resistive switching in TiO2 and HfO2 devices," *J. Vac. Sci. Technol*. vol. B34 (012202), 2016

Memristor *Device Types* & *Properties*

Device Variability!!!







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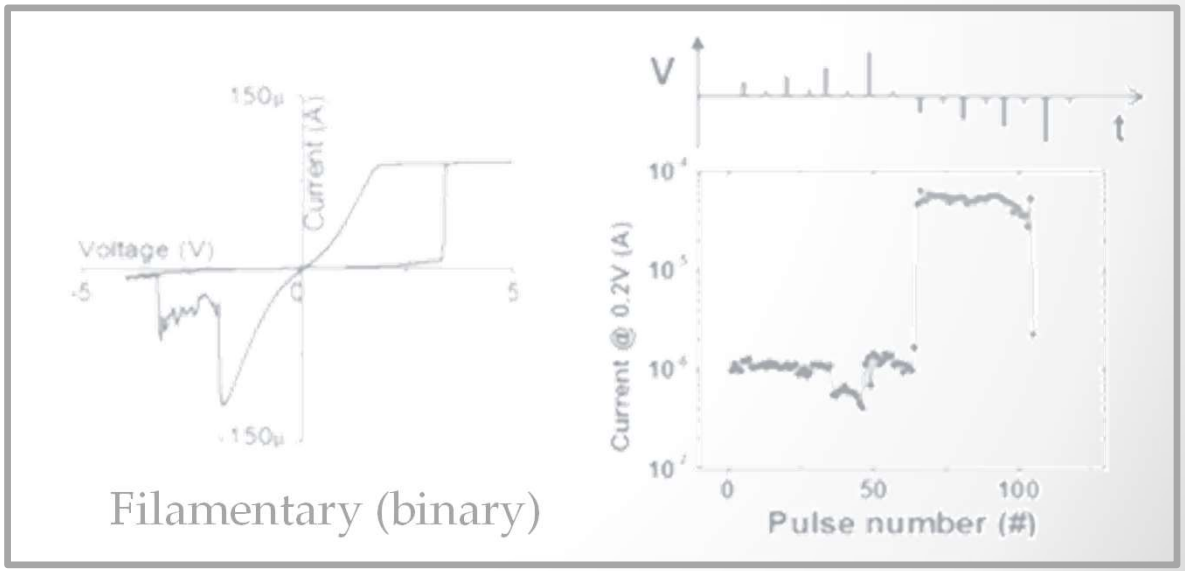


Filamentary (binary)

First Model by HP

$$\begin{cases} v = \mathcal{R}(w,i)\,i \\ \dfrac{dw}{dt} = f(w,i) \end{cases}$$

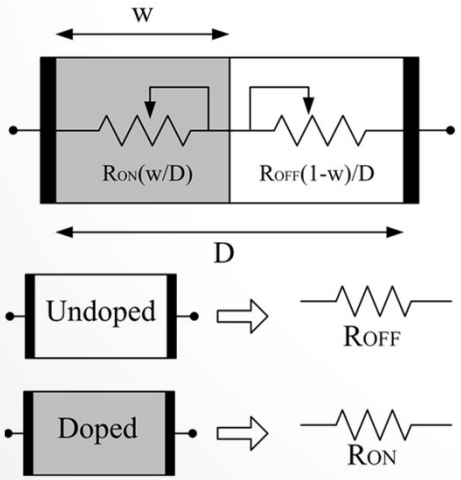
$$\begin{cases} v(t) = \left(\mathcal{R}_{ON}\dfrac{w(t)}{D} + \mathcal{R}_{OFF}\left(1-\dfrac{w(t)}{D}\right)\right) i(t) \\ \dfrac{dw(t)}{dt} = \mu_V \dfrac{\mathcal{R}_{ON}}{D}\, i(t) \\ w(t) = \mu_V \dfrac{\mathcal{R}_{ON}}{D}\, q(t) \end{cases}$$

$V = \mu \mathcal{E}$ (microelectronic carrier transport)

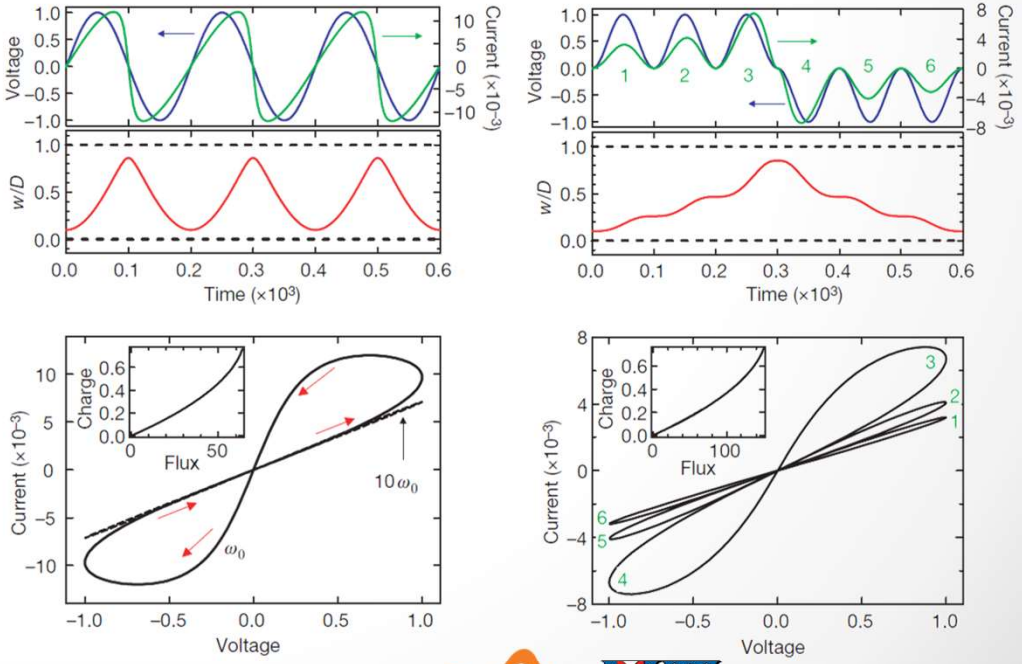
$\dfrac{dw(t)}{dt} = \mu_V \dfrac{V(t)}{D}$ $\left(\mathcal{E} = \dfrac{V}{L}\right)$

$\dfrac{dw(t)}{dt} = \mu_V \dfrac{R_{ON} \cdot I(t)}{D}$ ($V = IR$ Ohm's Law)

$\dfrac{dw(t)}{dt} = \mu_V \dfrac{R_{ON}}{D} \dfrac{dq(t)}{dt}$ $\left(I = \dfrac{dq}{dt}\right)$



Linear ionic drift in uniform field



More *precise* Models

This model is based on the phenomenon of *quantum tunneling*

$$i = G(w,v)v$$

and

$$\dot{w} = f(w,i).$$

off switching ($i>0$):

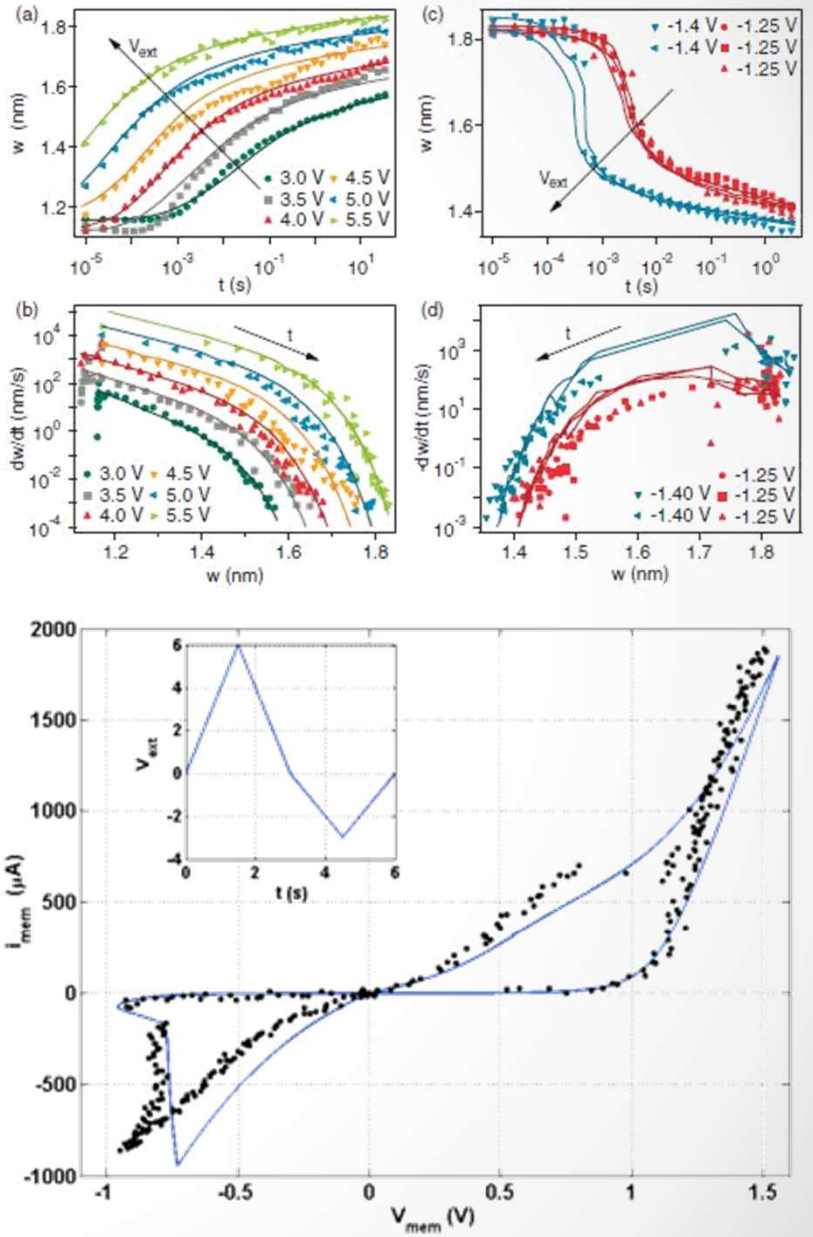
$$\dot{w} = f_{\text{off}} \sinh\left(\frac{i}{i_{\text{off}}}\right) \exp\left[-\exp\left(\frac{w-a_{\text{off}}}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right]$$

and the fitting parameters $f_{\text{off}}=3.5\pm1$ μm/s, $i_{\text{off}}=115\pm4$ μA, $a_{\text{off}}=1.20\pm0.02$ nm, $b=500\pm70$ μA, and $w_c=107\pm4$ pm;

on switching ($i<0$):

$$\dot{w} = f_{\text{on}} \sinh\left(\frac{i}{i_{\text{on}}}\right) \exp\left[-\exp\left(-\frac{w-a_{\text{on}}}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right]$$

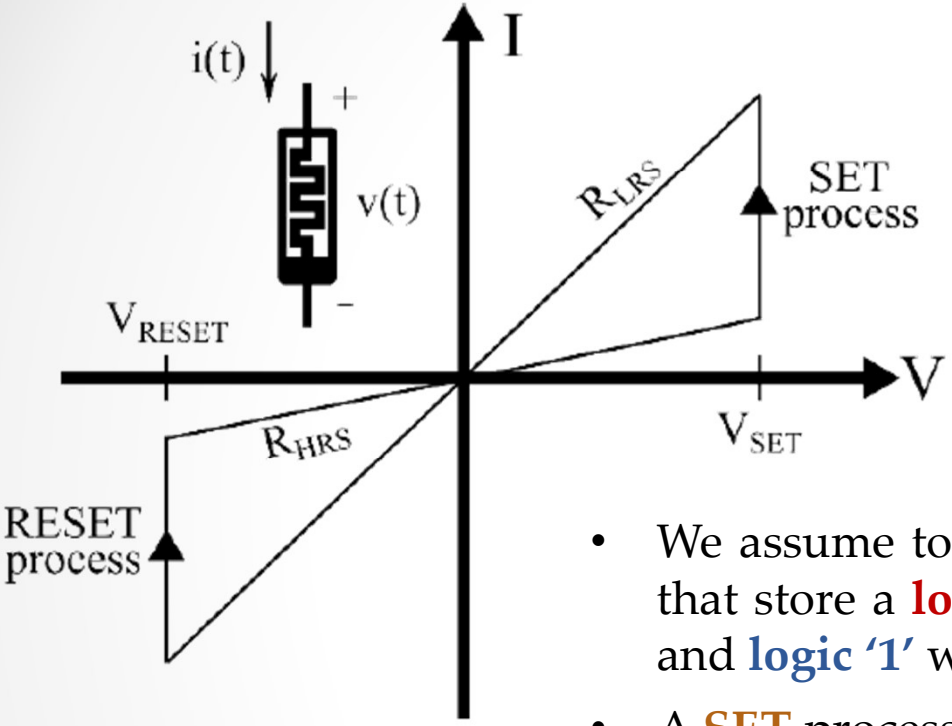
and the fitting parameters $f_{\text{on}}=40\pm10$ μm/s, $i_{\text{on}}=8.9\pm0.3$ μA, $a_{\text{on}}=1.80\pm0.01$ nm, $b=500\pm90$ μA, and $w_c=107\pm3$ pm

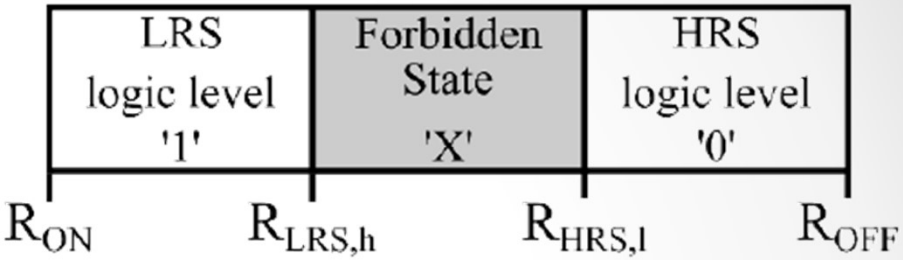


M. D. Pickett *et al.*, "Switching dynamics in titanium dioxide memristive devices," *J. Appl. Phys.*, vol. 106, no. 074508, pp. 1–6, 2009

Terminology & Assumptions

for memristor operation





- We assume to be using **threshold-type switching** memristors that store a **logic '0'** with a high resistive state (R_{OFF} or **HRS**) and **logic '1'** with a low resistive state (R_{ON} or **LRS**).
- A **SET** process (HRS→LRS) occurs when the device is **forward biased** with a voltage of amplitude higher than a V_{SET} threshold.
- A **RESET** process (LRS→HRS) occurs when it is **reverse-biased** with a voltage amplitude higher than a $|V_{RESET}|$ threshold.
- The thick line in the memristor symbol defines **polarity**.

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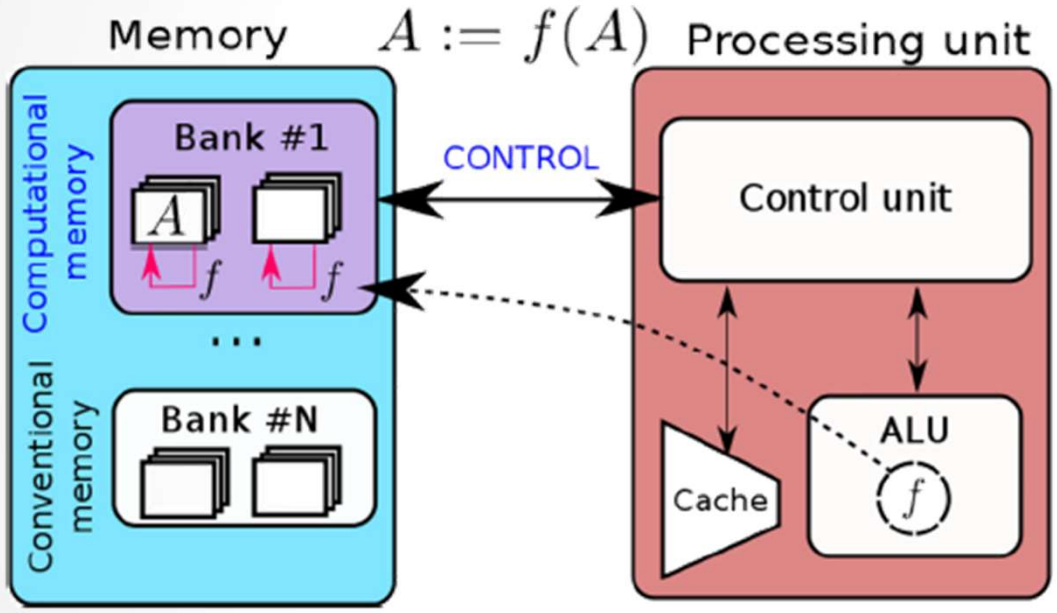
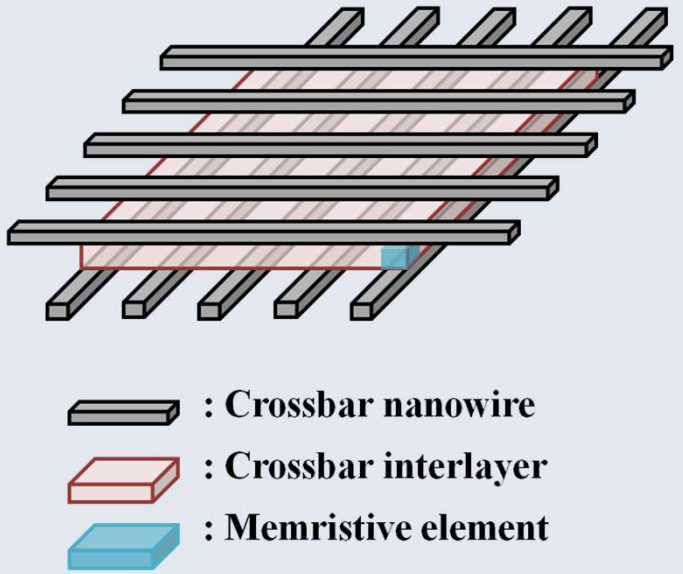
Motivation for *in Memory Logic*

- To build more powerful & energy-efficient computers, we need to **transition to novel architectures** where memory and processing are better collocated.





Memristors are considered the key enabling technology for **computational memories**

- The idea would be to build computing units where **memory and processing co-exist**
- "In-memory computation" can be performed with the **applied voltages driving the memristive logic circuits**, implemented directly in the cross-point cells.

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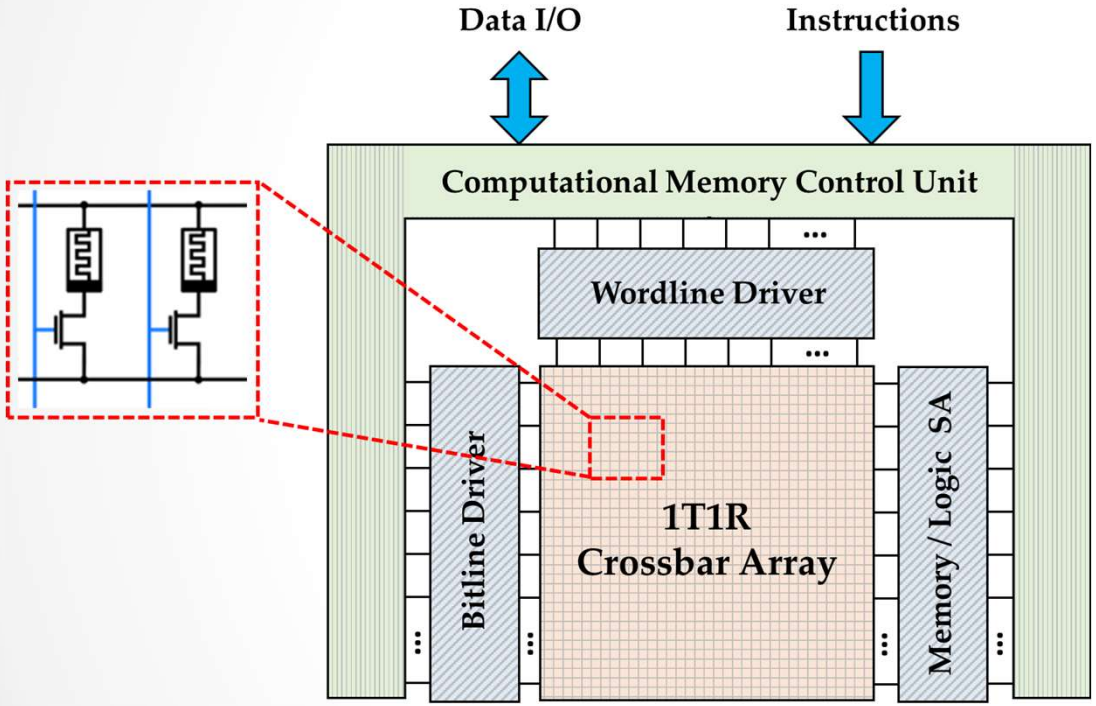

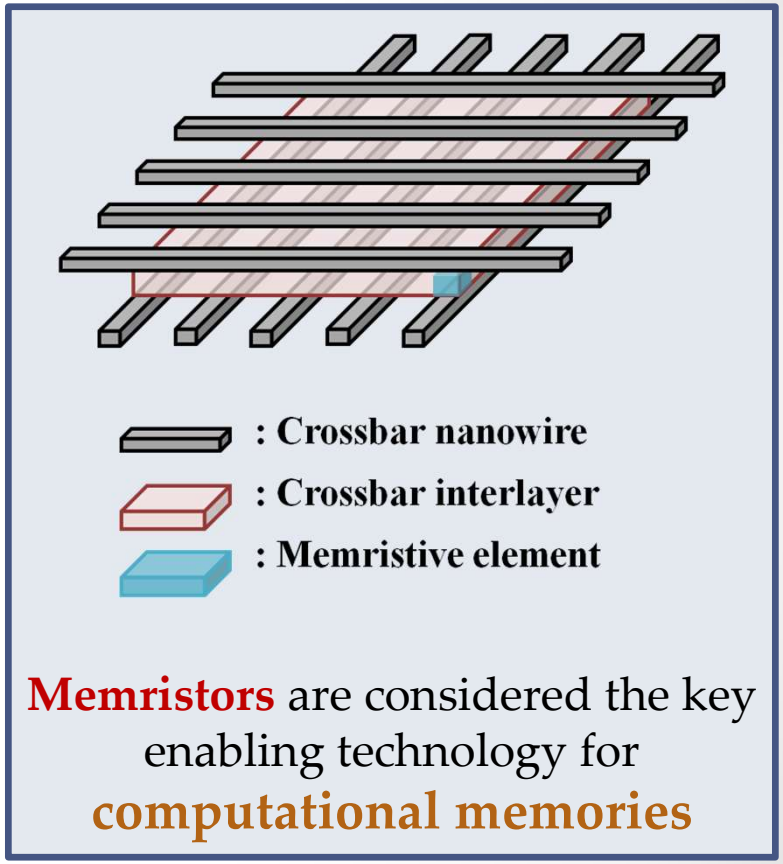

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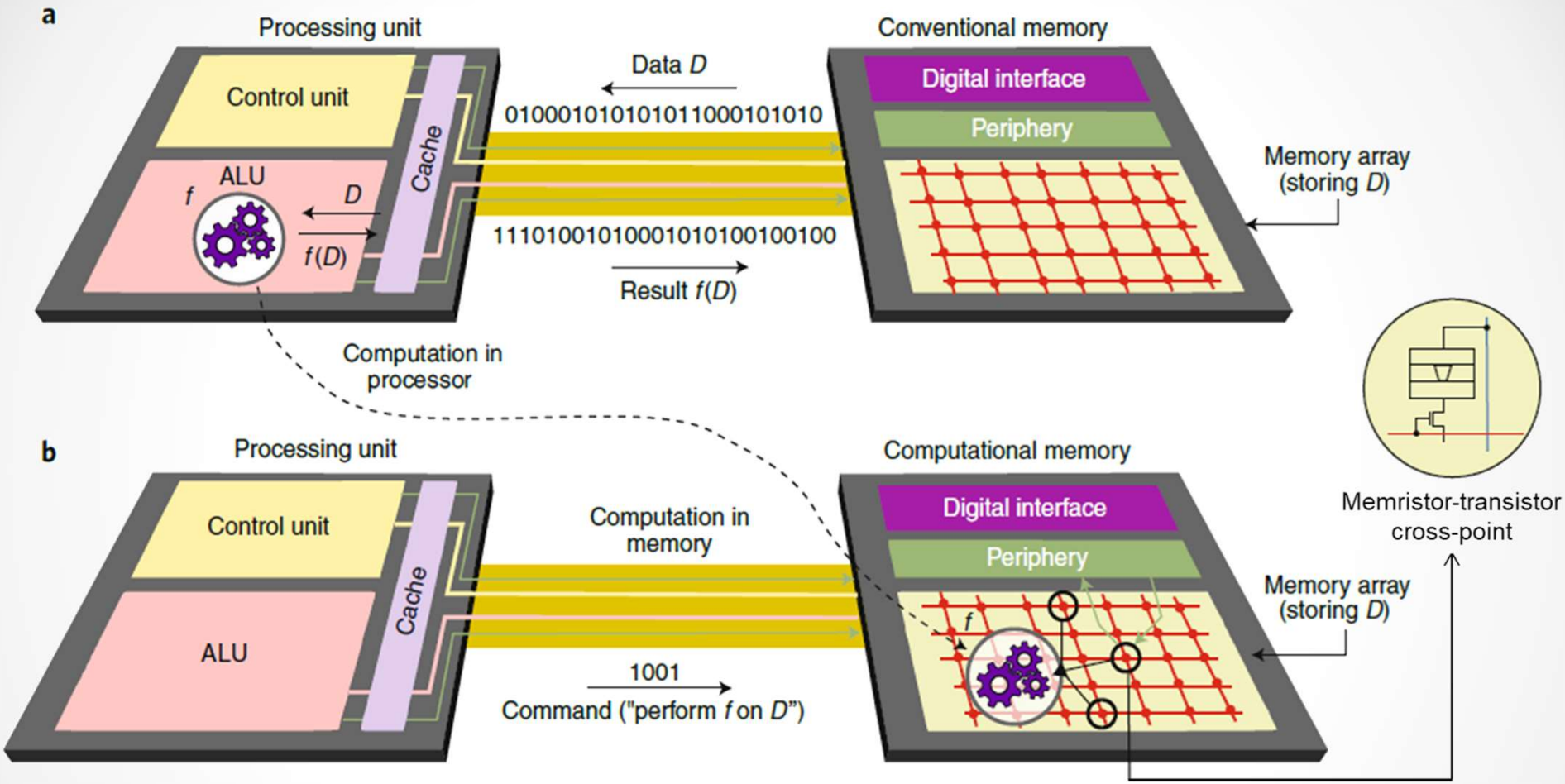


"Memory devices and applications for in-memory computing," *Nat. Nanotechnol.*, vol. 15, pp. 529–544, 2020

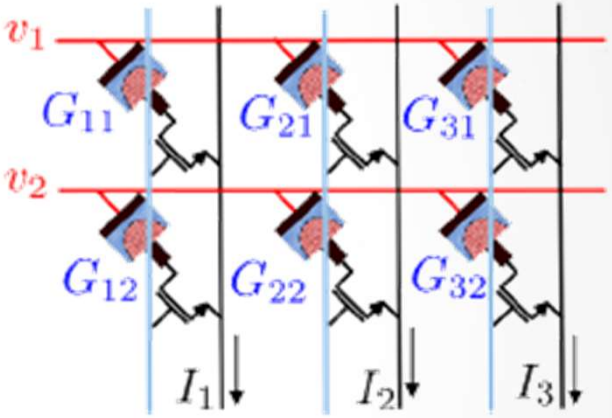
- "In-memory computation" can be performed with the **applied voltages driving the memristive logic circuits**, implemented directly in the cross-point cells.

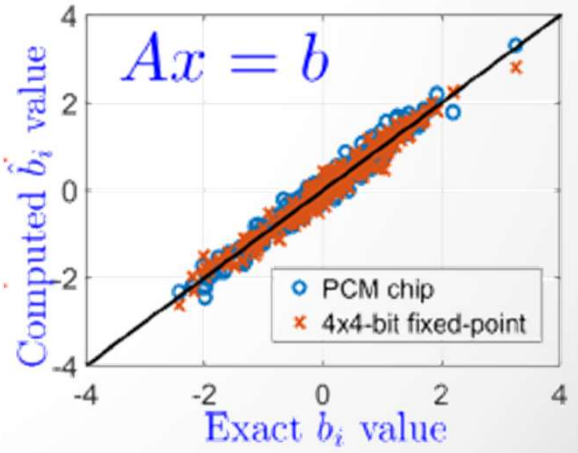
Potential of a *Computational Memory*

J. Appl. Phys. 124, 111101 (2018)

- **A key attribute** of brain-inspired computing is the **co-location of memory and processing**.
- To realize computation exactly at the place where the data are stored.
- One arithmetic operation that can be realized is **matrix-vector multiplication**.
  - The elements of **A should be mapped linearly to the conductance** values of memristors
  - The **x values** are encoded into the **amplitudes of voltages** applied along the rows.
  - The resulting **currents** along the columns will be **proportional to the result b**.

$$\begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \\ A_{31} & A_{32} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix}$$

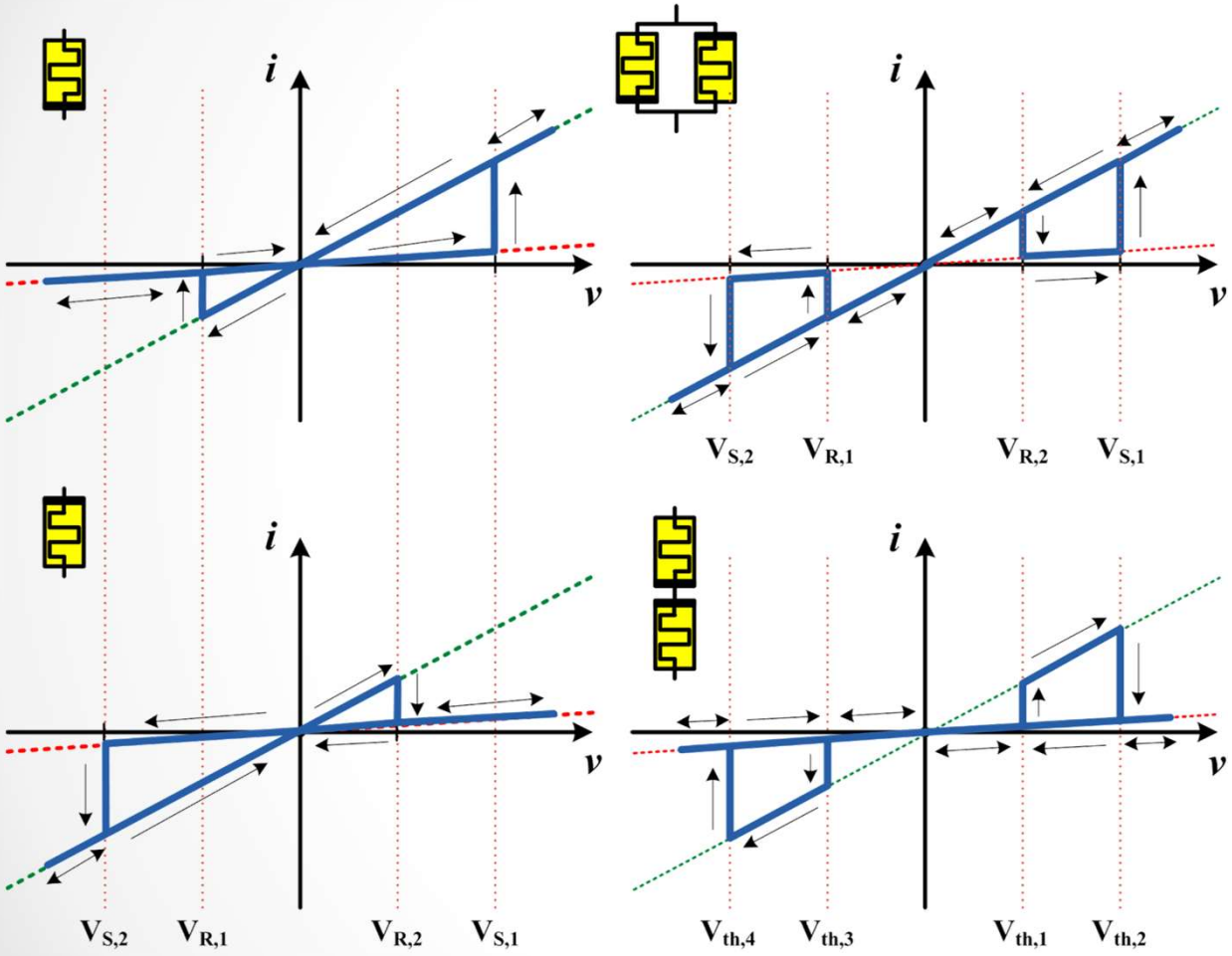




Matrix-vector multiplication can be performed with O(1) complexity

Modeling Collective Switching Behavior

A positive/negative voltage applied to the top terminal with respect to the **bottom terminal** (denoted by the **black thick line**) always tends to decrease/increase the memristance.

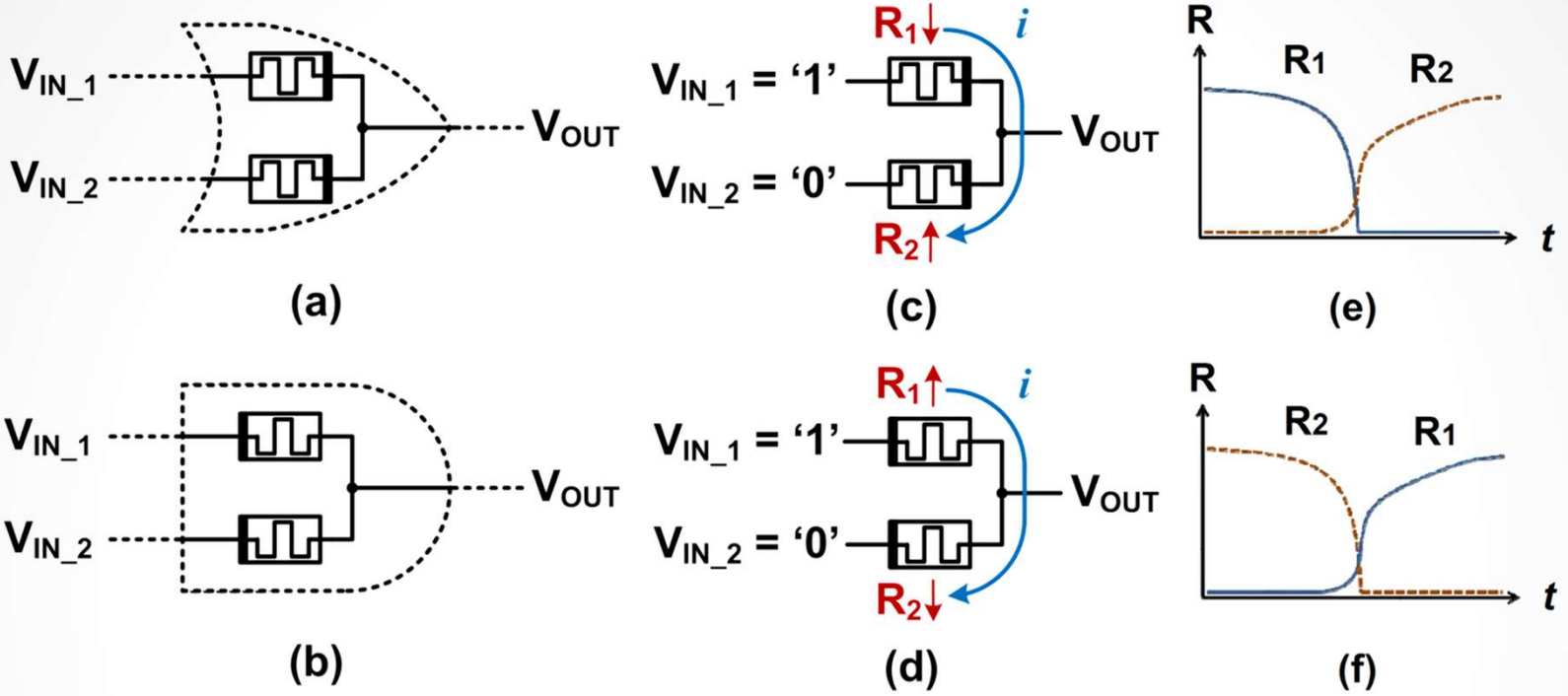


Memristors with opposite polarities present reversed (**flipped**) ***i–v* characteristic**

The *threshold*-based response of memristors resembles that of two-state switches, "allowing" (i.e. being more conductive) or "preventing" (i.e. being less conductive) the current flow in a circuit branch

Simultaneously biased memristors when arranged in a **complementary** manner will be changing their states in a **reciprocal way**

MRL : Memristor Ratio-ed Logic



Main properties

- It relies on memristors in series with opposite polarity (voltage divider)
- The output node is the common node
- Memristive AND/OR logic gates
- CMOS NOT gate is required for signal inversion and restoration

Circuit design limitations

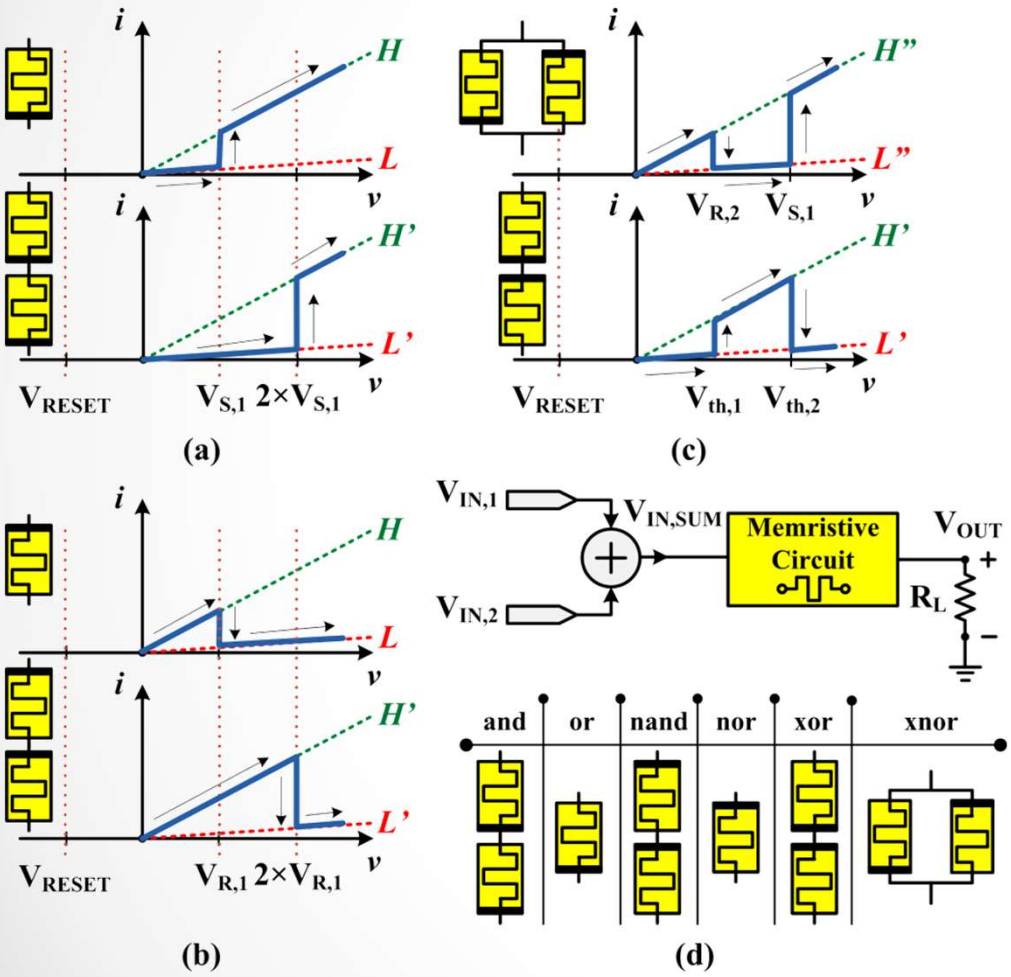
- Inputs & output are voltage signals

Memristors do not hold data

S. Kvatinsky, N. Wald, G. Satat, A. Kolodny, U. C. Weiser and E. G. Friedman, "MRL - Memristor Ratioed Logic," 2012 *Int. Workshop on Cellular Nanoscale Netw. and Appl.* (*CNNA*), Turin, Italy, Aug. 29 – 31

Another Ratio-ed Logic Scheme

The total conductance is inherently suitable for Boolean logic operations



Input signal correspondence

0V ↔ '0' and $V_{th1} < V_o < V_{th2}$ ↔ '1'

$$OR: G(V_{IN,SUM} = V_{IN,1} + V_{IN,2}) = \begin{cases} H, V_{IN,SUM} > V_{S,1} \\ L, \quad otherwise \end{cases}$$

$$AND: G(V_{IN,SUM} = V_{IN,1} + V_{IN,2}) = \begin{cases} H', V_{IN,SUM} > 2 \times V_{S,1} \\ L', \quad otherwise \end{cases}$$

$$XOR: G(V_{IN,SUM} = V_{IN,1} + V_{IN,2}) = \begin{cases} H', V_{th,1} < V_{IN,SUM} < V_{th,2} \\ L', \quad otherwise \end{cases}$$

$$XNOR: G(V_{IN,SUM} = V_{IN,1} + V_{IN,2}) = \begin{cases} H'', V_{R,2} < V_{IN,SUM} < V_{S,1} \\ L'', \quad otherwise \end{cases}$$

$\{L, H\} = \{G_{ON}, G_{OFF}\}$

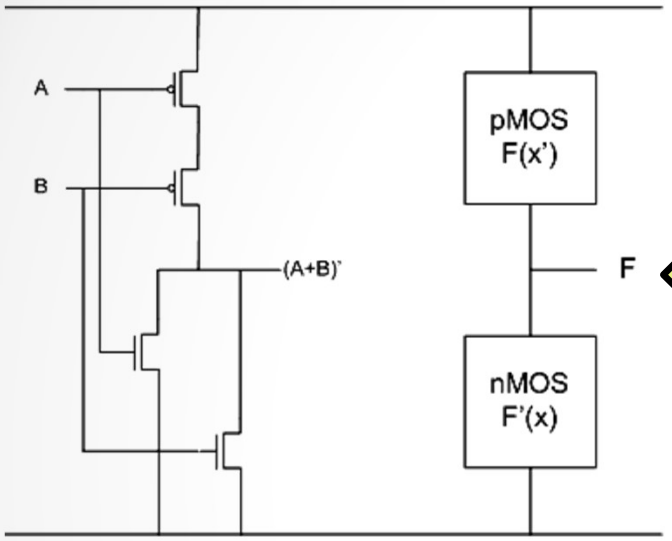
$\{L', H'\} = \{2 \times G_{ON}, 2 \times G_{OFF}\}$

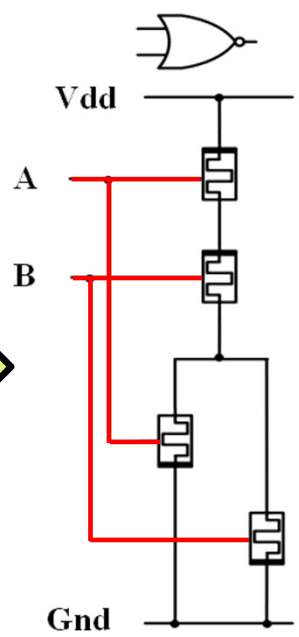
$\{L'', H''\} = \{½ \times G_{ON}, ½ \times G_{OFF}\}$

Memristors do not hold data

I. Vourkas and G. Ch. Sirakoulis, "Emerging Memristor-based Logic Circuit Design Approaches: A Review," *IEEE Circ. and Syst. Mag*, vol. 16, no. 3 (3rd quarter), pp. 15-30, 2016

Memristive CMOS-*like* Circuit Operation

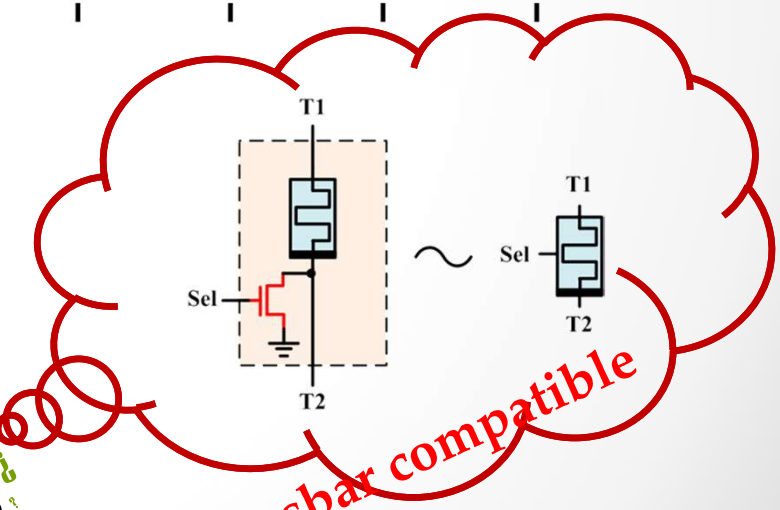




Initial State	AB 00	AB 01	AB 11	AB 10
OFF	ON	ON	OFF	OFF
OFF	ON	OFF	OFF	ON
ON	OFF	OFF	ON	ON
ON	OFF	ON	ON	OFF

Circuit design limitations

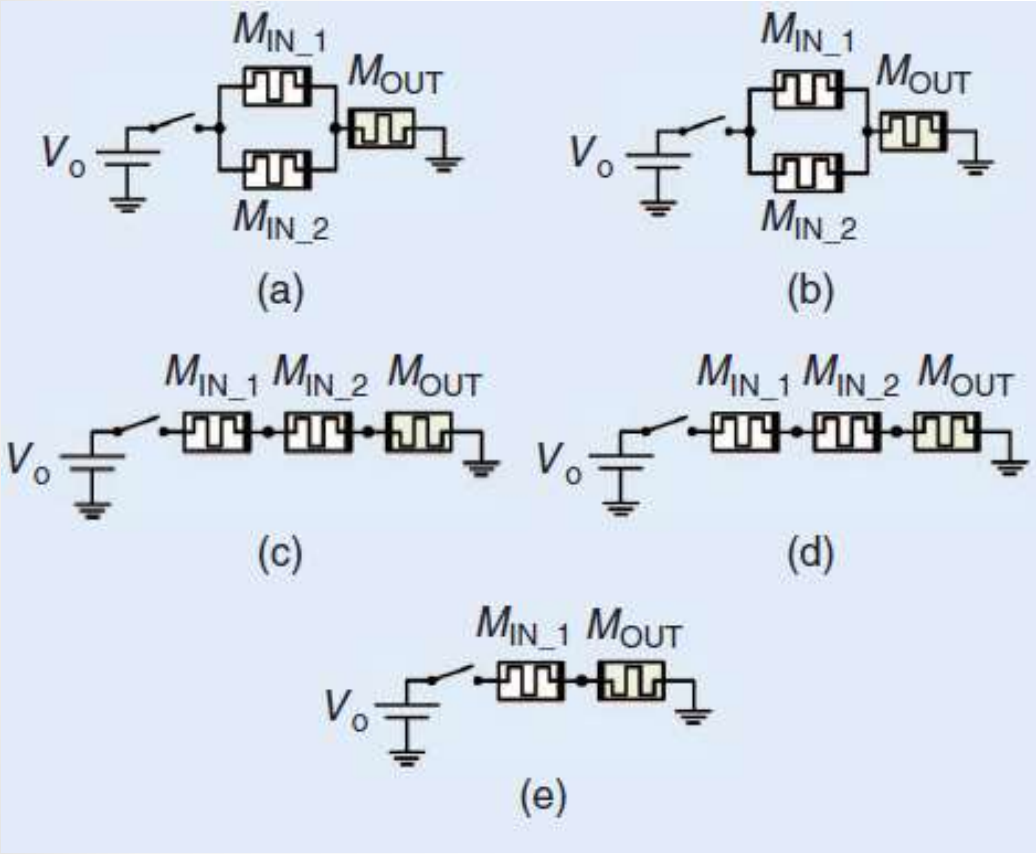
- Sequential application of inputs
- Interconnect complexity
- Requires 2x memristors to store data



"A Novel Design and Modeling Paradigm for Memristor-based Crossbar Circuits", *IEEE Trans. Nanotechnology*, vol. 11, no. 6, pp. 1151-1159, 2012

Conditionally Switching Logic: Examples

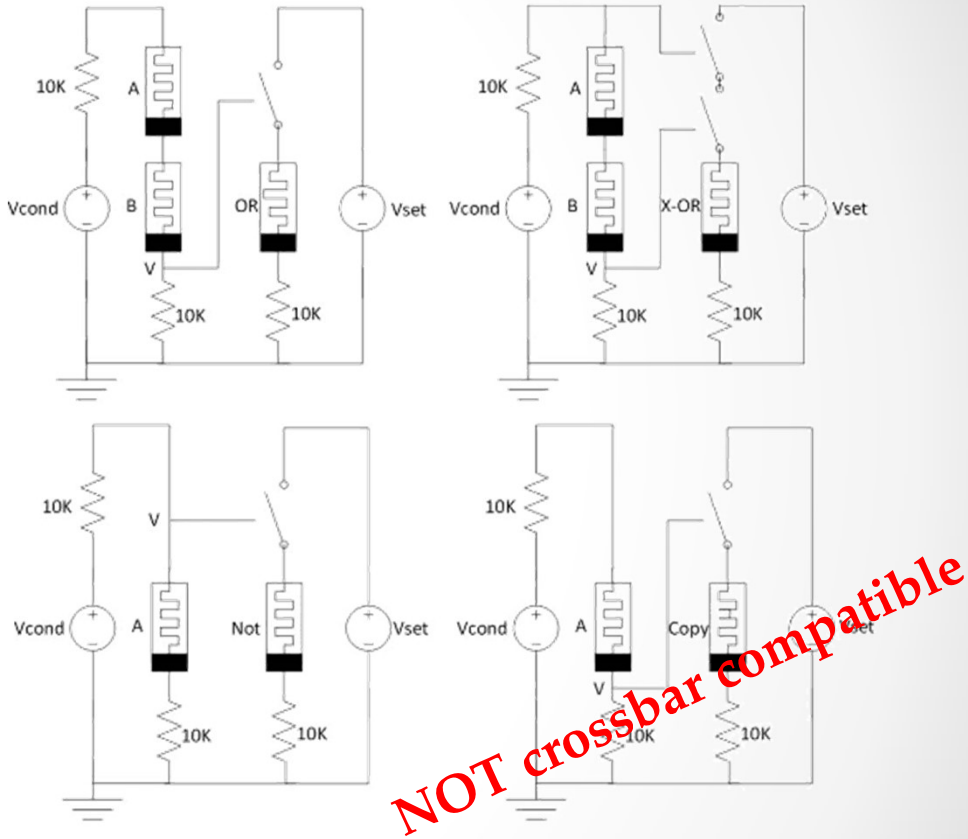
Memristor Aided Logic (MAGIC)



(a) Circuit schematic of a two-input (a) NOR , (b) OR , (c) NAND , (d) AND , and (e) a NOT (CRS) MAGIC logic gate

S. Kvatinsky, *et al.*, "MAGIC: Memristor aided LoGIC," *IEEE Trans. Circuits Syst. II*, vol. 61, no. 11, pp. 895–899, 2014

Memristor as Driver (MAD)

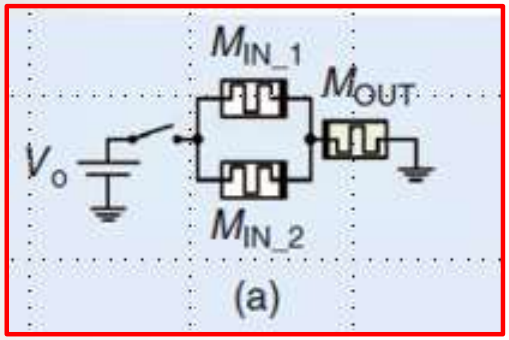


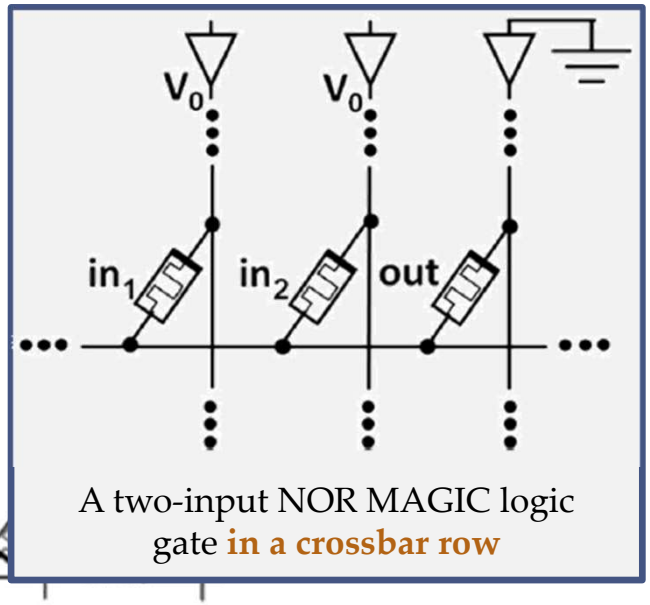
MAD implementation for OR, XOR, NOT, and COPY gates.

L. Guckert, *et al.*, "MAD Gates—Memristor Logic Design Using Driver Circuitry," *IEEE Trans. Circuits Syst. II*, vol. 64, no. 2, pp. 171–175, 2017

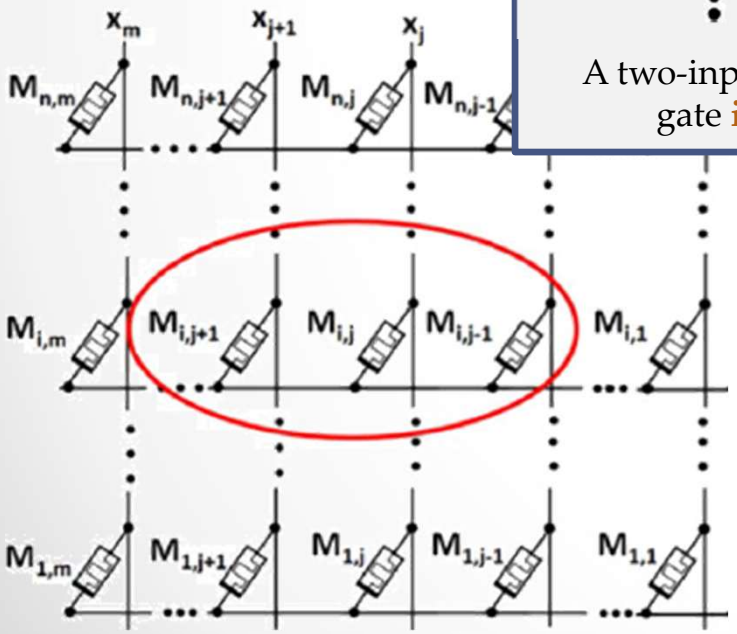
Conditionally Switching Logic: MAGIC

Memristor Aided Logic (MAGIC)

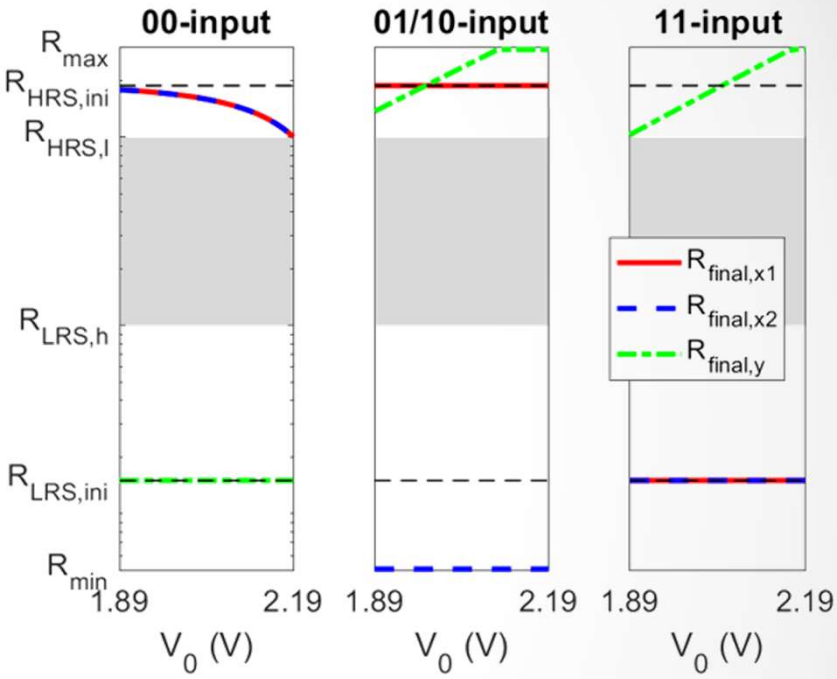




A two-input NOR MAGIC logic gate **in a crossbar row**



Design Space Limitations



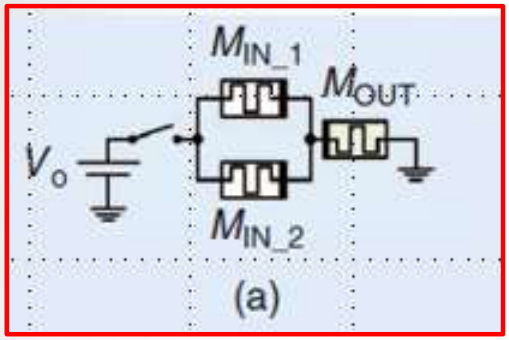
- Input voltage requirements for MAGIC NOR are as follows:

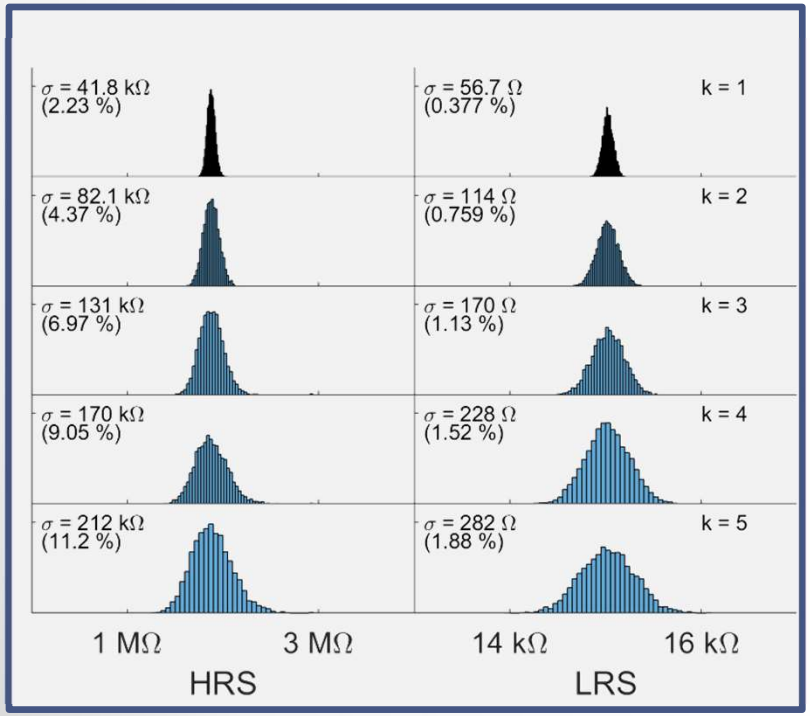
$$2\times|V_{RESET}| < V_0 < V_{SET}$$

M Escudero, *et al.*, "Memristive logic in crossbar memory arrays: Variability-aware design for higher reliability," *IEEE Trans. Nanotechnol.* 18, 635-646, 2019

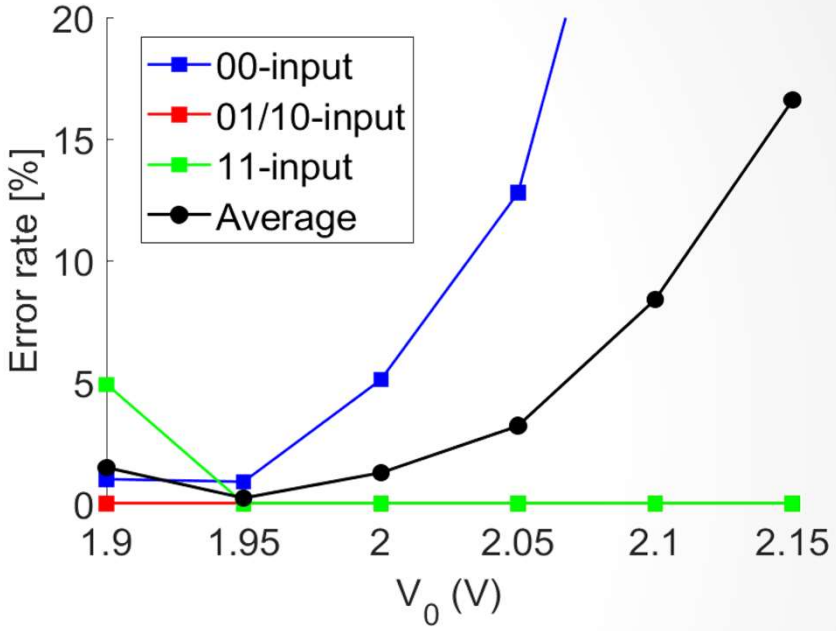
Conditionally Switching Logic: MAGIC

Memristor Aided Logic (MAGIC)





Impact of Variability



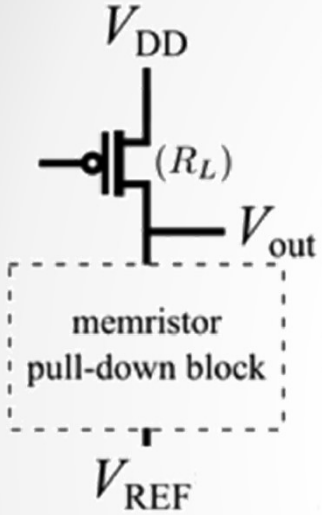
- Correctness of the logic computations is degraded in the presence of device variability

Z. Jiang, H. Li, J. H. Engel, S. Yu, and X. Guan, "Stanford-PKU RRAM Model v2.0.0," [Online]. Available: https://nano.stanford.edu/stanfordrram-model

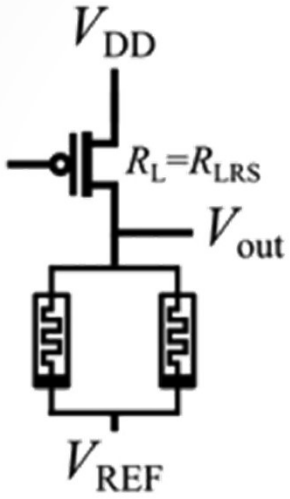
M Escudero, *et al.*, "Memristive logic in crossbar memory arrays: Variability-aware design for higher reliability," *IEEE Trans. Nanotechnol.* 18, 635-646, 2019

Ratioed combinational circuit design

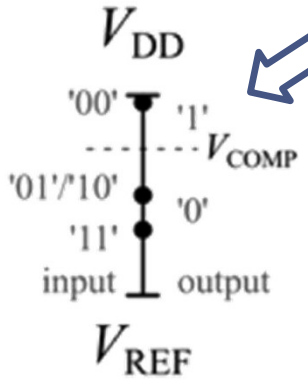
a *solution* for memristive *in-memory* computing



(a)



(b)



(c)

$$V_{out} = V_{REF} + (V_{DD} - V_{REF}) \frac{R_{eq}}{R_L + R_{eq}}$$

a) General NOR/NOT gate topology

b) Example of 2-input NOR gate topology

c) Noise margins for reading logic 1 or logic 0 at the output node

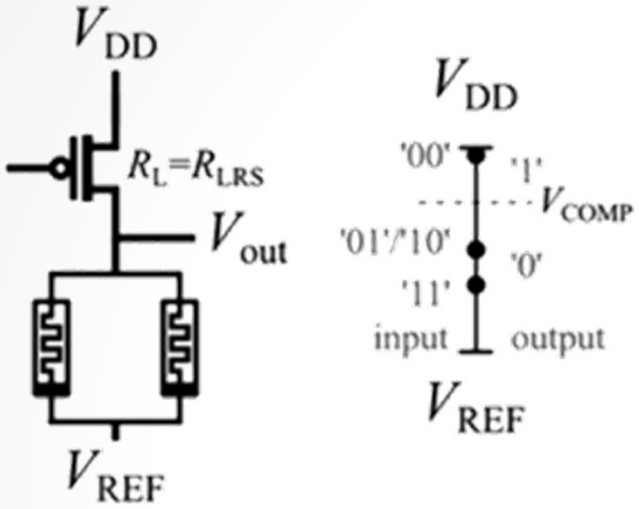
TABLE I
RATIOED LOGIC NOR2

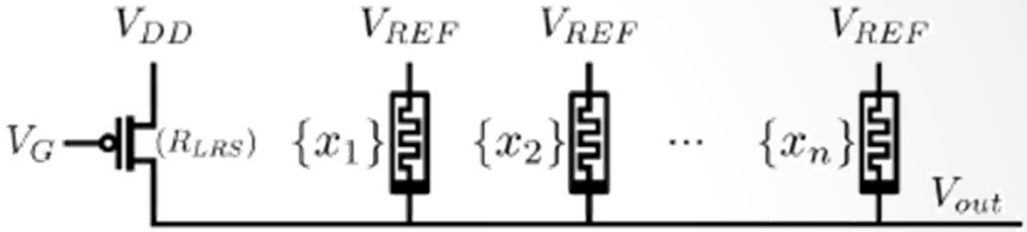
Input logic combination	R_{eq} of input memristors	Expected V_{out} value	Logic Output
"00"	$R_{HRS}/2$	$\approx V_{DD}$	'1'
"01"/"10"	$\approx R_{LRS}$	$V_{REF} + (V_{DD}-V_{REF})/2$	'0'
"11"	$R_{LRS}/2$	$V_{REF} + (V_{DD}-V_{REF})/3$	'0'

C. Fernandez, and I. Vourkas, "ReRAM-based Ratioed Combinational Circuit Design: a Solution for in-Memory Computing," 2020 Int. Conf. on Modern Circuits and Syst. Technol. (MOCAST), Bremen, Germany, Sept. 07-09

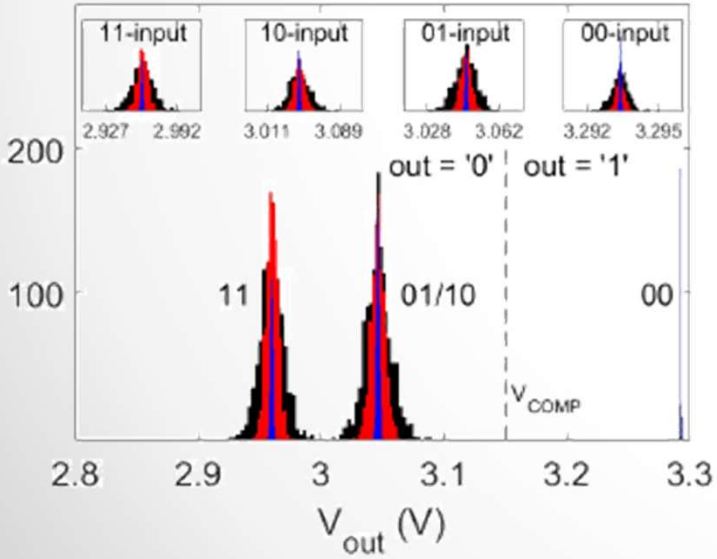
Ratioed combinational circuit design

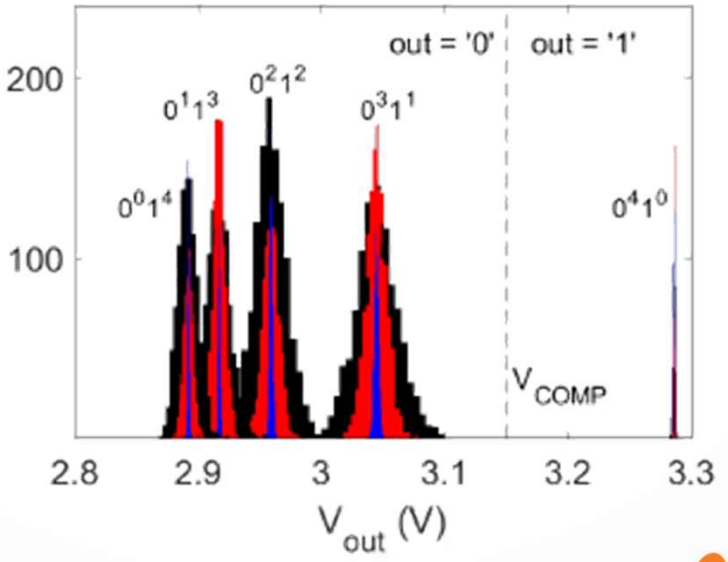
A design highly robust against memristor device variability

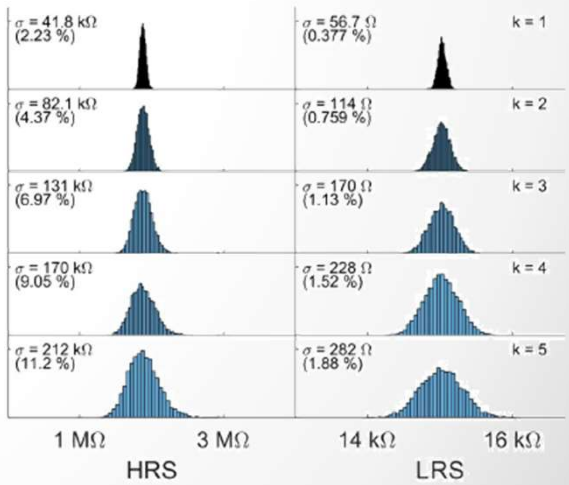




Histograms of *V*out for NOR*n* after the evaluation of 1000 operations for each possible input combination





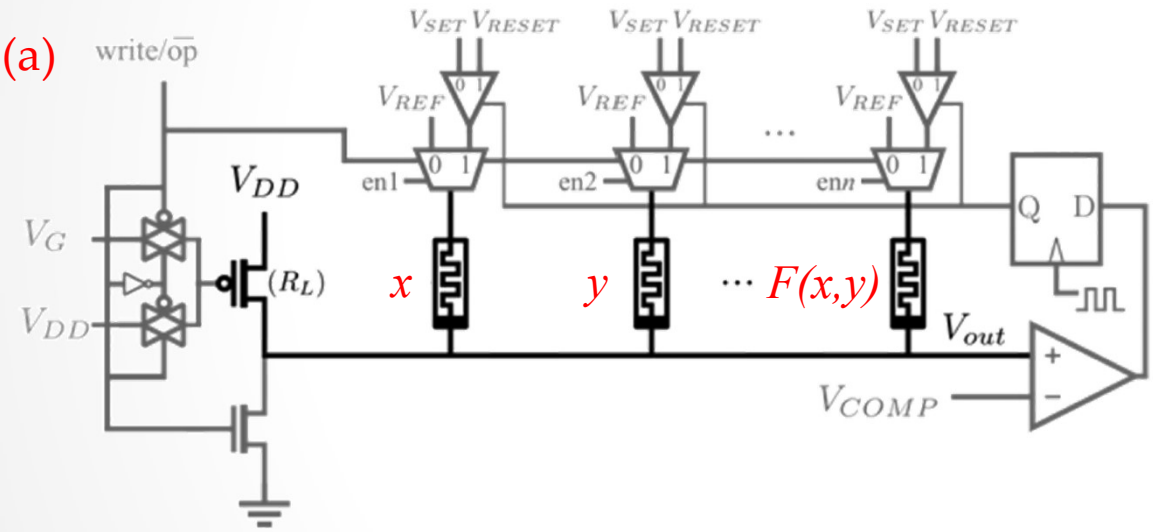


Ratioed combinational circuit design

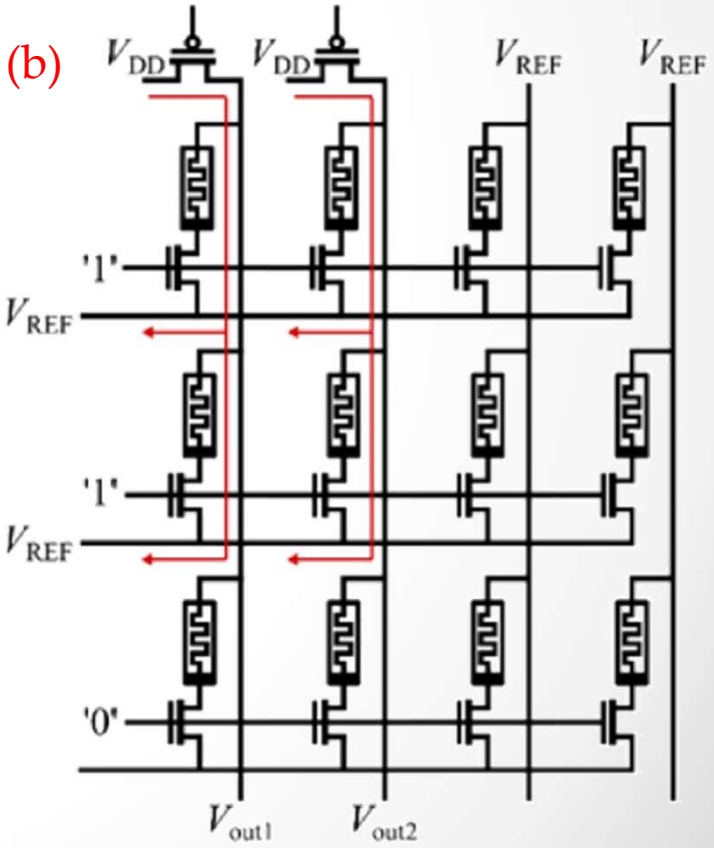
Details of the underlying ReRAM architecture

- We assume a memristor-transistor (1T-1R) ReRAM hardware structure
- We designed the **peripheral circuitry of the controller** for such a 1T-1R **computational memory** supporting ratioed logic

(a)



(b)



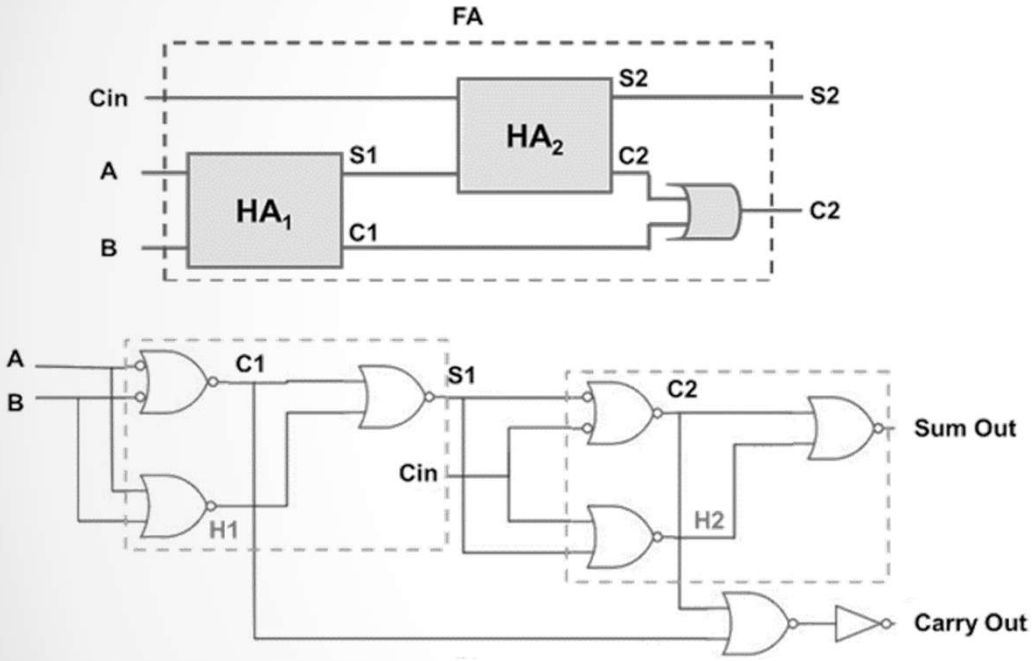
a) Simplified memory driving circuitry shown for one crossbar array row (wordline).

b) Extension for a $n \times m$ crossbar array. Example shows pulsing for two parallel NOR2 computations

Logic circuit simulated in LTSPICE

1-bit Full Adder implemented in *chained* NOR logic

A **decomposed FA** in a multi-level circuit comprising two Half Adders (HA)



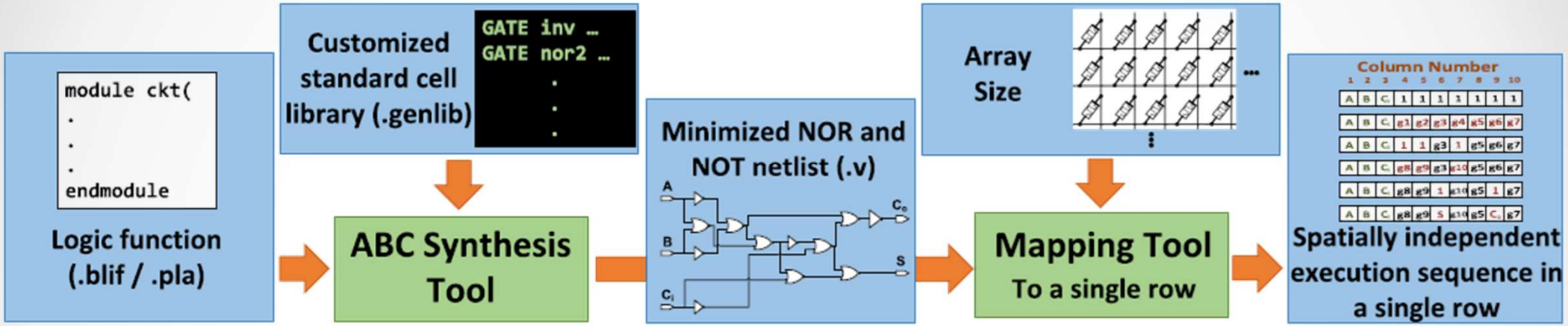
1-BIT FULL ADDER COMPUTING STEPS FOR RATIOED LOGIC

Step	Operation	M1	M2	M3	M4	M5
0	*INIT*	***A***	***B***			***Cin***
1	*(M1)NOR(M2) →M3*	A	B	$H1$		Cin
2	*NOT(M1) →M1*	$\bar{A}$	B	$H1$		Cin
3	$NOT(M2) \rightarrow M2$	$\bar{A}$	$\bar{B}$	$H1$		Cin
4	$(M1)NOR(M2) \rightarrow M4$			$H1$	$C1$	Cin
5	$(M3)NOR(M4) \rightarrow M1$	$S1$			$C1$	Cin
6	$COPY(M5) \rightarrow M2$	$S1$	Cin		$C1$	
7	$COPY(M4) \rightarrow M5$	$S1$	Cin			$C1$
8	*(M1)NOR(M2) →M3*	$S1$	Cin	$H2$		$C1$
9	*NOT(M1) →M1*	$\overline{S1}$	Cin	$H2$		$C1$
10	$NOT(M2) \rightarrow M2$	$\overline{S1}$	$\overline{Cin}$	$H2$		$C1$
11	$(M1)NOR(M2) \rightarrow M4$			$H2$	$C2$	$C1$
12	$(M3)NOR(M4) \rightarrow M1$	*Sum Out*			$C2$	$C1$
13	*NOT((M4)NOR(M5)) →M2*	***Sum Out***	***Carry Out***			

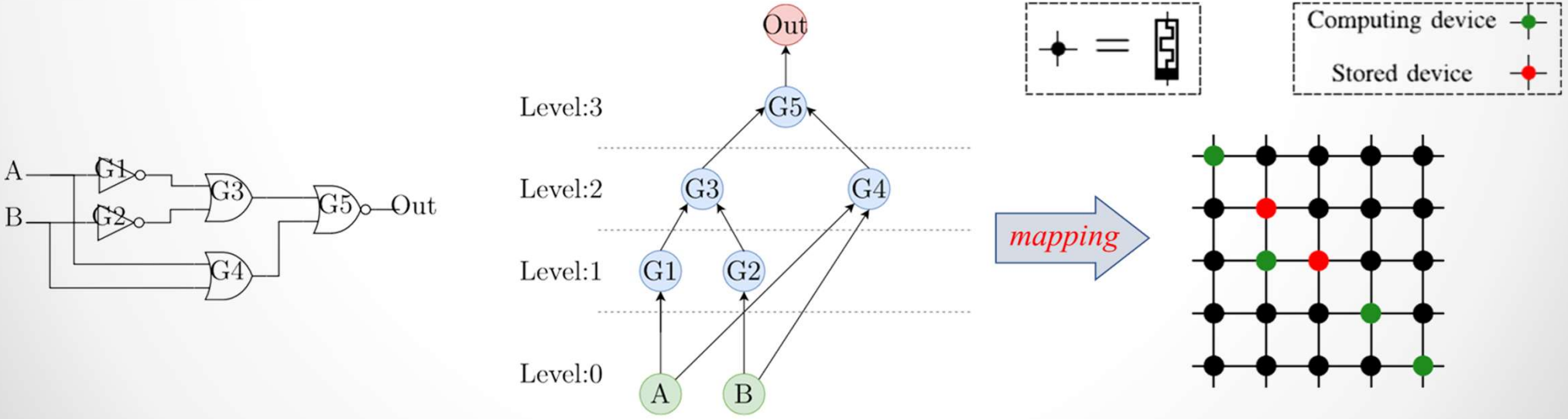
C. Fernandez, and I. Vourkas, "ReRAM-based Ratioed Combinational Circuit Design: a Solution for in-Memory Computing," 2020 Int. Conf. on Modern Circuits and Syst. Technol. (MOCAST), Bremen, Germany, Sept. 07-09

Synthesis for ReRAM Computing

spatio-temporal properties of the multi-level logic operations



DOI: 10.1109/TCAD.2019.2931188



(a) (b) (c)

Outline

Introduction to memristors

- The memristor as the forth fundamental circuit element
- Device types & most important properties
- Modeling of memristors

Memristor-based logic

- Motivation for in memory logic with memristors
- Logic styles based on conditional switching of memristors
- Details of ratioed logic style robust to device variability

Experimental work with commercial memristors

- Related industry examples
- Ad-hoc instrumentation tools and basic circuit topologies
- Examples of measured device behavior
- Opportunities for collaboration

Related Industry *chasing the AI space*

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IP Licensing

Crossbar RRAM technology is available as non-volatile, low latency, low power embedded memory IP blocks.

3D RRAM

Crossbar RRAM low latency, high-density memory chips are in the works and hold the promise of how storage will be redefined.

Consumer Electronics

Enterprise Storage

Industrial/Auto/Medical

Internet of Things

Mobile Computing

Wearables

Related Industry *chasing the AI space*

Reconfigurable In-Memory Computing Chips

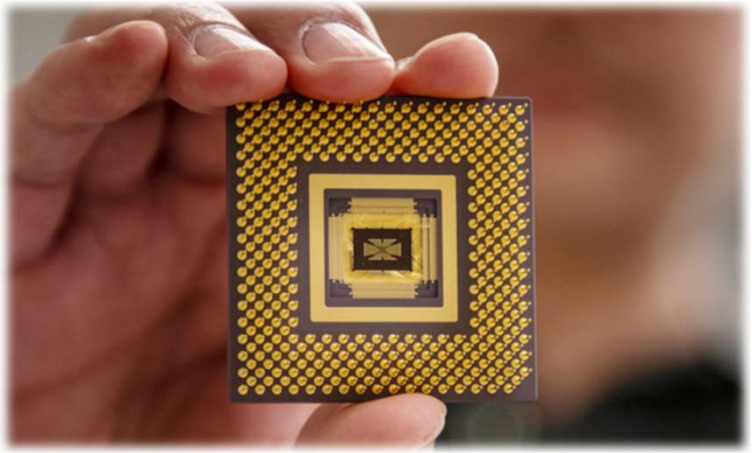
IEEE SPECTRUM

31 Jul 2019 | 12:00 GMT

MEMRYX

First Programmable Memristor Computer

Michigan team builds memristors atop standard CMOS logic to demo a system that can do a variety of edge computing AI tasks



Speaking of *devices* commercially available

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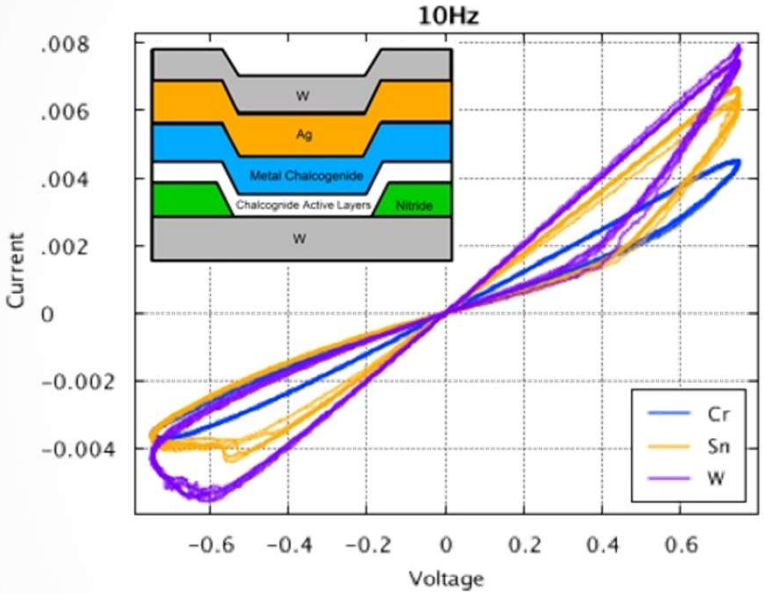
KNOWM MEMRISTORS – W, CR, SN



Electrical Differences

- Switching Speed
- Endurance
- Data Retention
- On and Off Resistance States
- Incremental "Nudging" Sensitivity

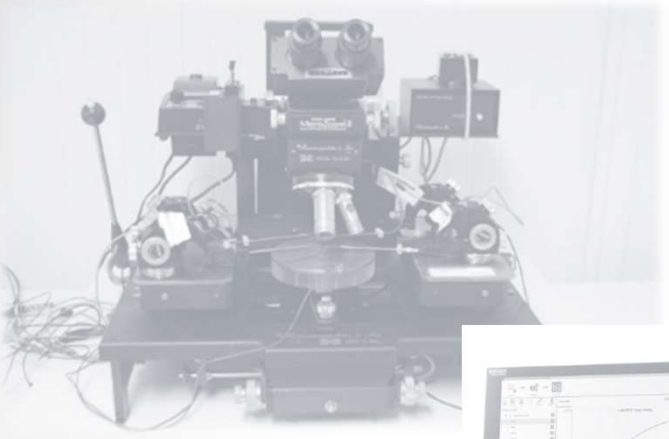
Physical Differences

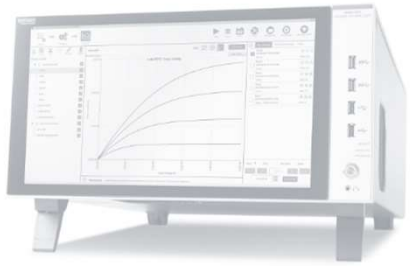
- Doping Material in Active Chalcogenide Layer
- Phase Transition Temperature (>250 degrees Celsius)

KNOWM

Knowm W, Cr, and Sn Memristor Types

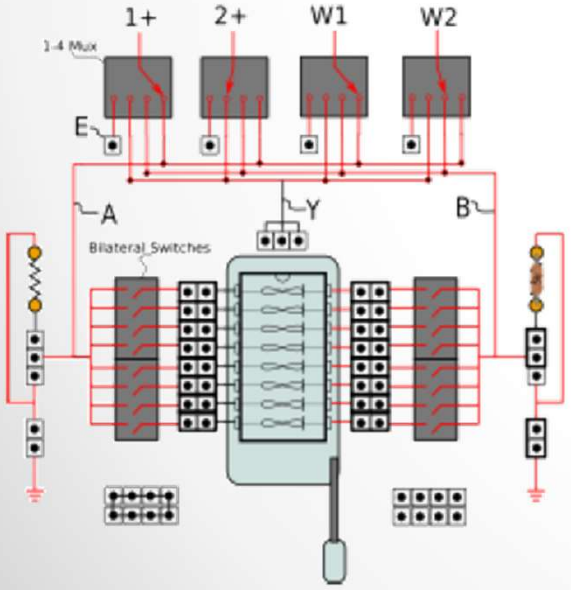
Speaking of *equipment*

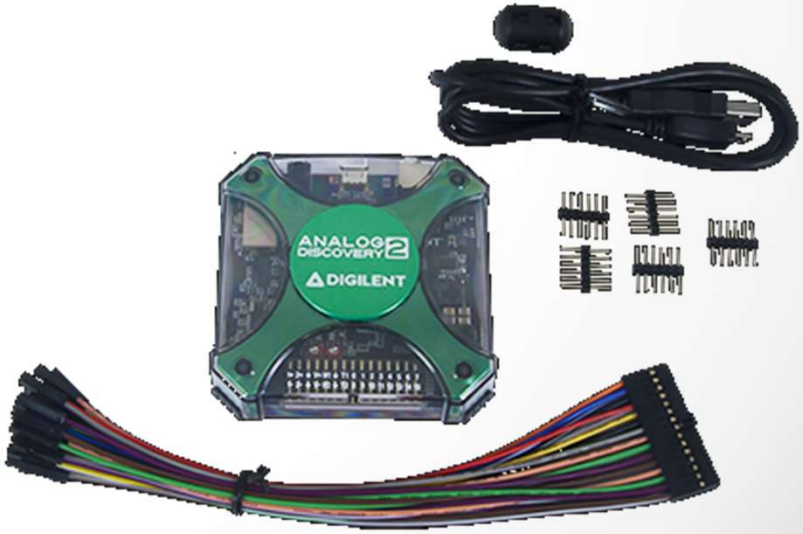




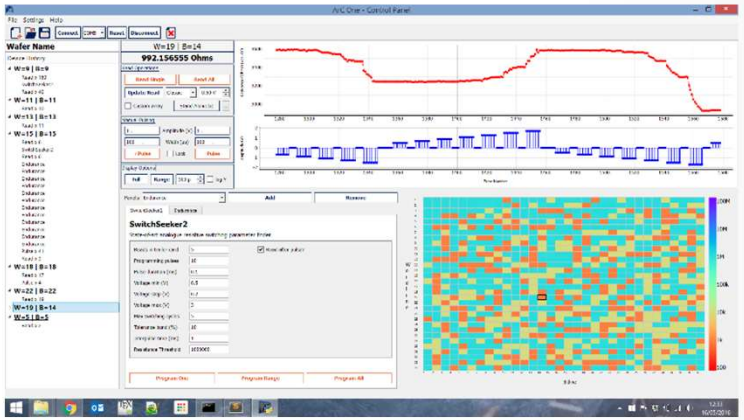
Using our imagination and perseverance, we can realize measurements using instrumentation solutions that cost a fraction of the cost of gold-standard equipment… and without the constraints of a Lab!

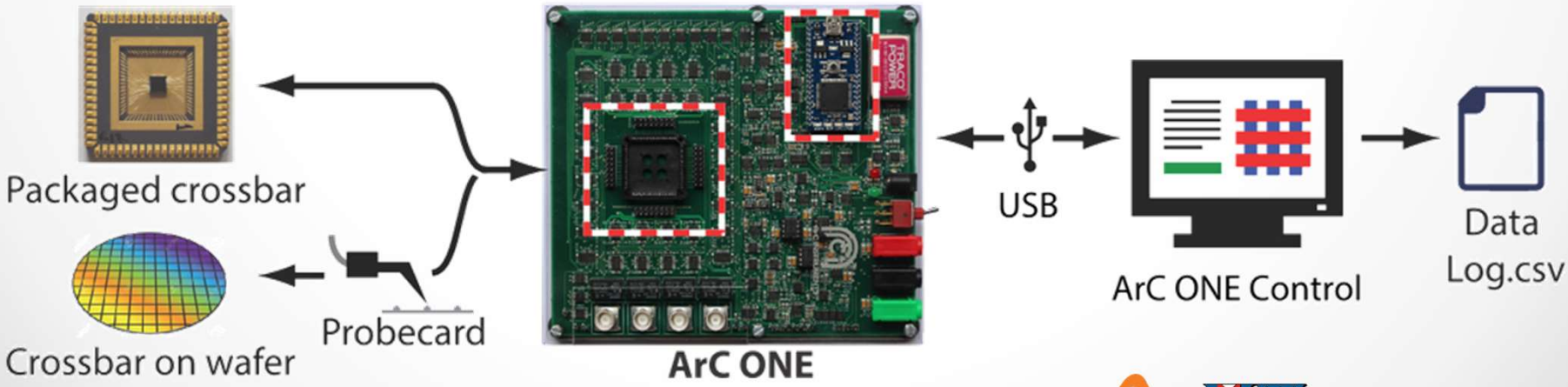
J. Gomez, *et al.*, "Experimental Measurements on Resistive Switching Devices: Gaining Hands-on Experience," *2018 Int. Conf. on Modern Circuits and Syst. Technol. (MOCAST)*, Thessaloniki, Greece,





More Tools developed for Memristors

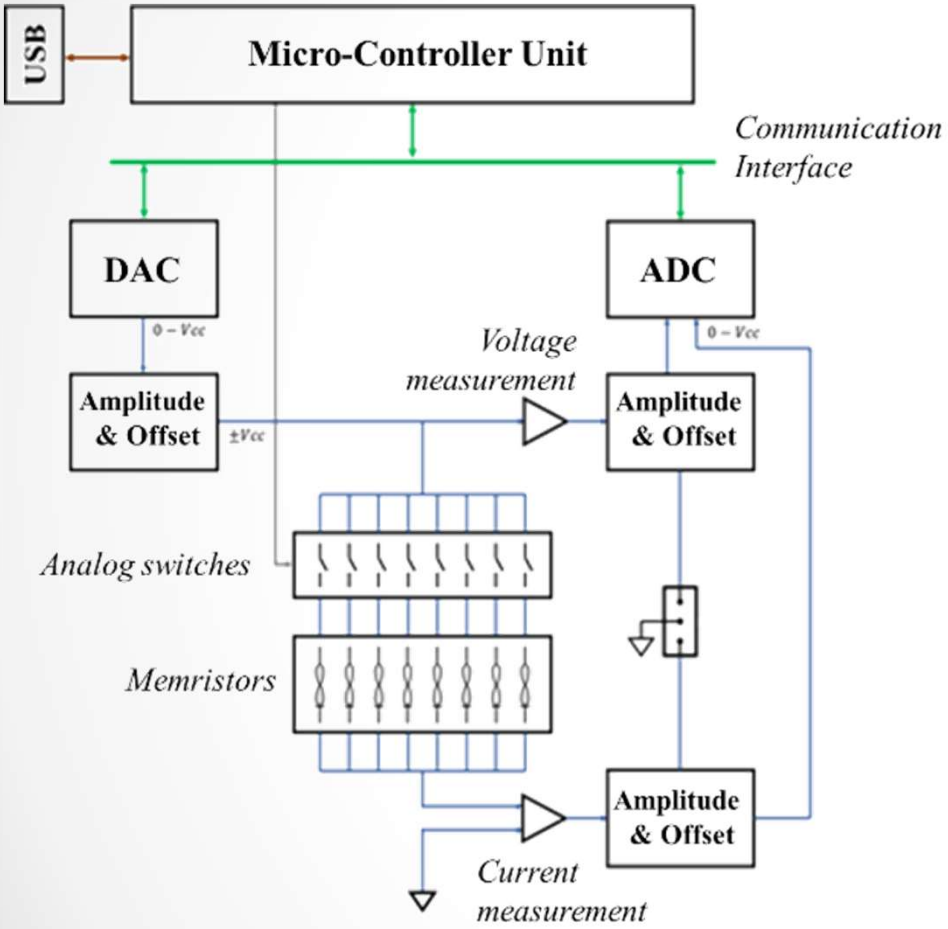




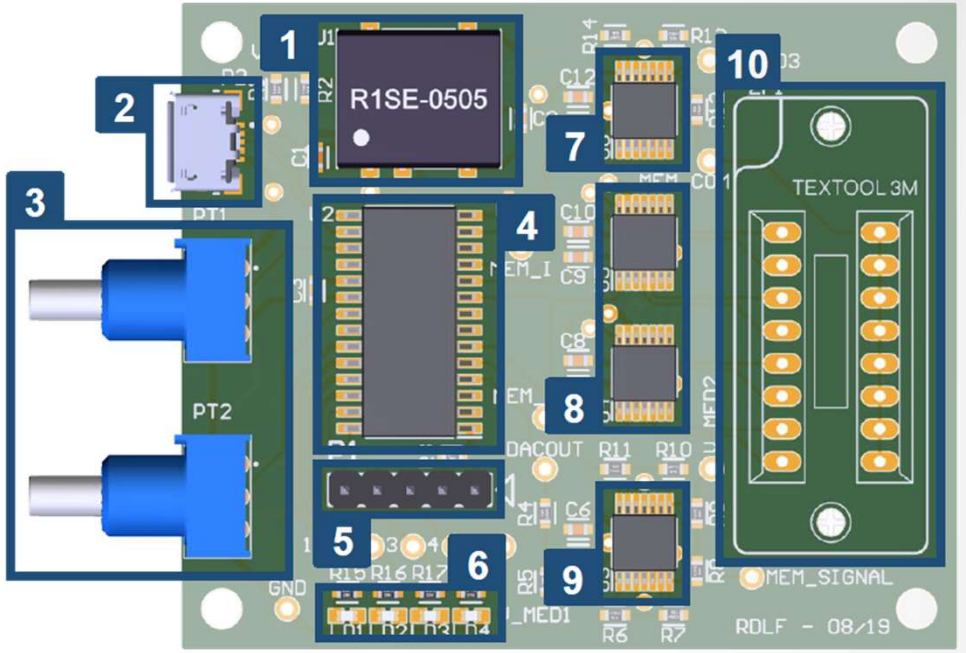
Create our own ad-hoc Tools

balancing cost with performance & utility

Generic block-level description



Top view of the board

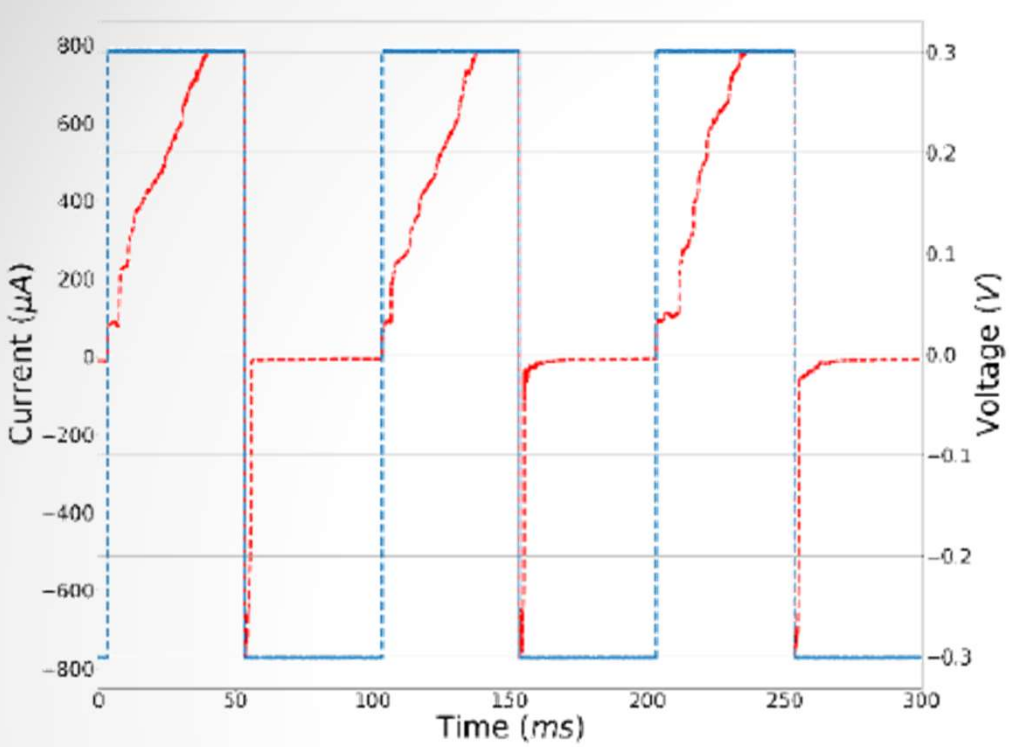


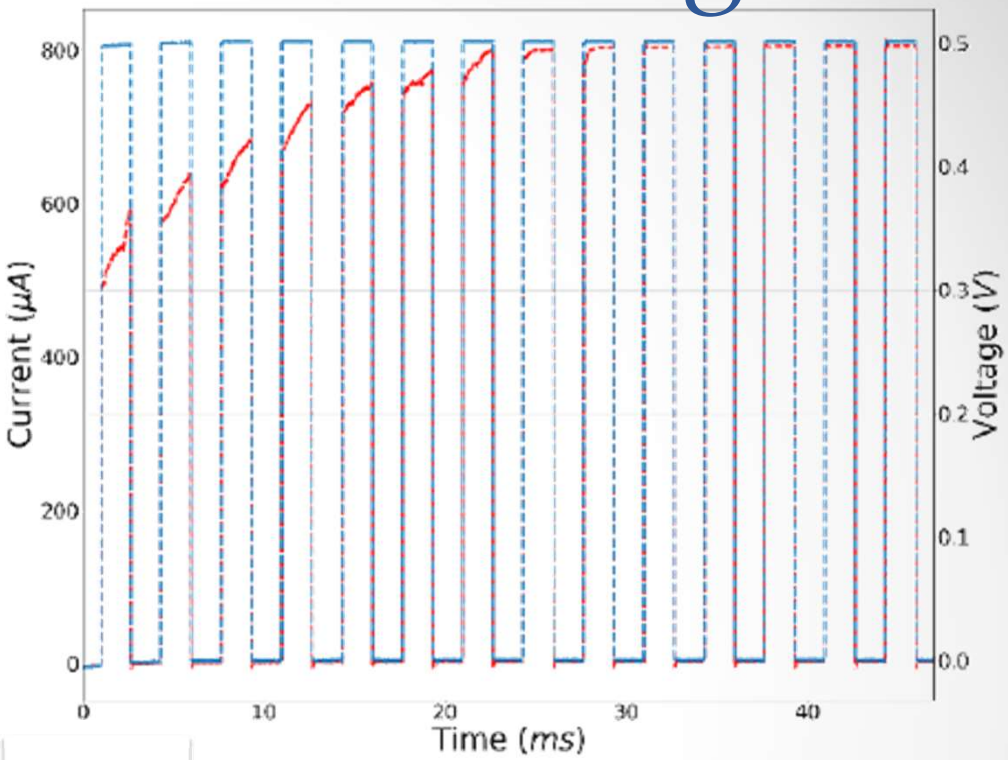
Highlighted parts

1. 5V voltage source
2. USB mini port
3. analog potentiometers
4. PIC MCU chip
5. ICSP connector
6. status LEDs
7. TS464CPT opamp for current measurement
8. ADG1604 MUXes
9. TS464CPT opamp for signal conditioning and voltage measurement
10. Zero-Insert-Force (ZIF) socket for DIP16 memristor chips

"On the development of MCU-based ad hoc HW interface circuitry for memristor characterization," 2020 *IEEE Eur. Conf. on Circuit Theory and Design* (*ECCTD*), Sofia, Bulgaria, 7-10 Sept.

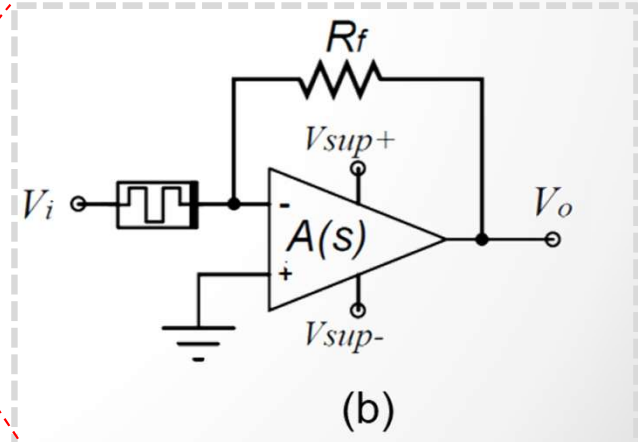
Multi-level Memristor Tuning





(transimpedance amplifier)

(a)

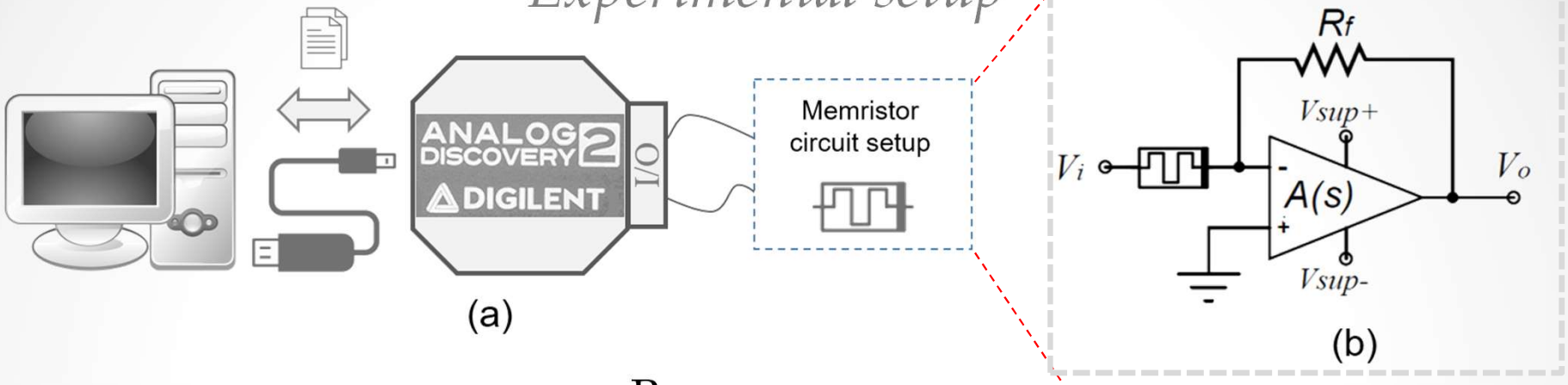


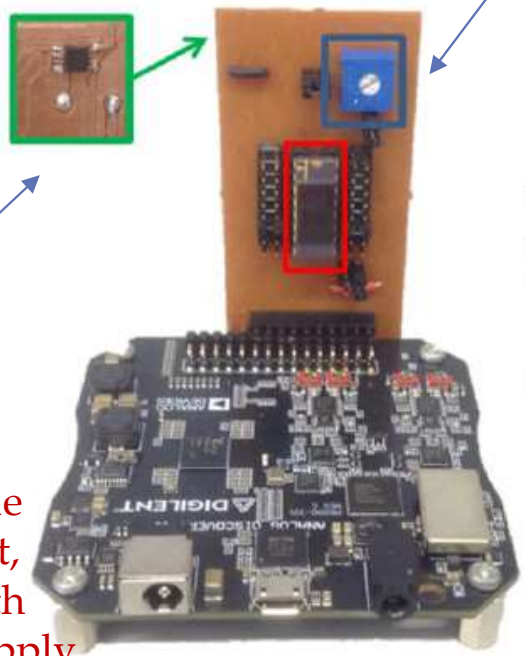
(b)

"Exploring Memristor Multi-Level Tuning Dependencies on the Applied Pulse Properties via a Low-Cost Instrumentation Setup", *IEEE Access*, vol. 7, pp. no. 1, pp. 59413 – 59421, 2019

Multi-level Memristor Tuning

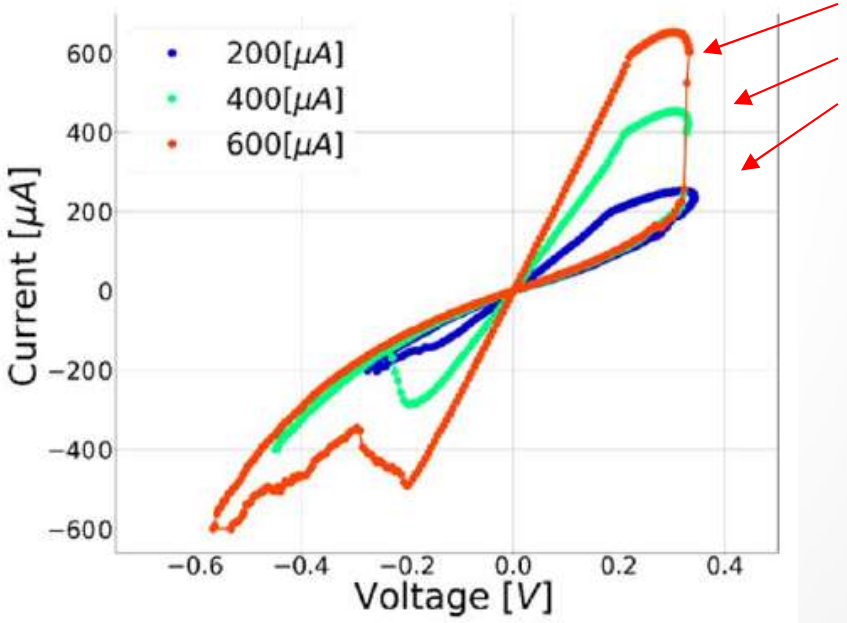
Experimental setup





MIC 7122YMM Opamp

(selected for its wide Vsup range support, also compatible with the ±5V voltage supply provided by the Digilent AD2)



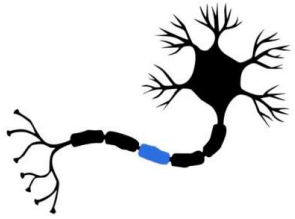
Such simple ideas

could have impact on industrial solutions

HOME PRODUCTS R&D AWARDS ABOUT US CONTACT

SOAP Layout V2b

Board specifications are



MEMRISTORS
APPLICATIONS
ELECTRONIC DESIGN

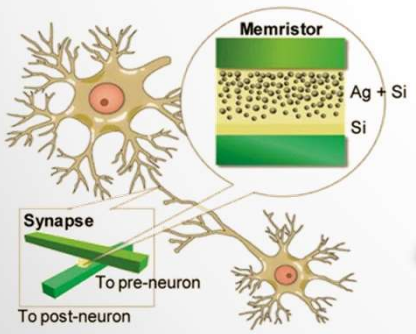
- Three configurations methods:
  - Classic Resistors (CONF1)
  - Transimpedance topology as described in DOI:10.1109/ACCESS.2019.2915100 (CONF2) https://ieeexplore.ieee.org/abstract/document/8708254
  - Bridge programming as described in DOI:10.1080/00207217.2019.1692371 (CONF3) https://doi.org/10.1080/00207217.2019.1692371
- Antiserial configuration allowed on 4 memristors
- Precise onboard measurement of Memristor's Voltage & Current
- Memristors & CONF/APP mode selection by Waveforms interface (AD2)

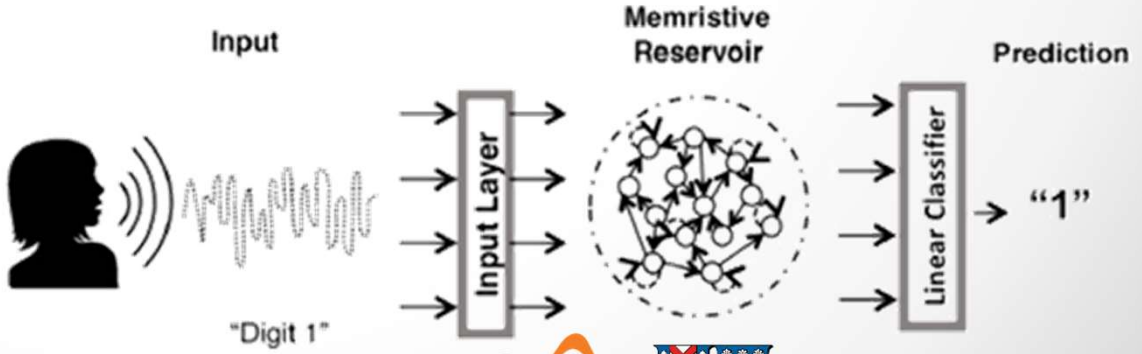
https://www.conceptualise.be/

Opportunities for Collaboration

- Artificial Neural Networks built with memristors
- Development of Instrumentation tools for memristor devices
- Unconventional & in-memory Computing Architectures
- Programmable and/or adaptive analog circuits with memristors
- Memristive sensors
- …

"Anyone who has never made a mistake, has never tried anything new." – Einstein





Technical University of Crete | SCHOOL OF ELECTRICAL & COMPUTER ENGINEERING

Thank you All for your kind attention!

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Questions ?

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