# Communications Hardware In The Post-Happy-Scaling Era

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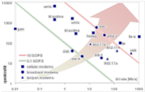
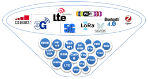
- C.-H. Chen, F. Sheikh (Intel Labs)

# The End of the "Happy Scaling" Era



Increasing DSP algorithm complexity.



Increasing need for flexibility.

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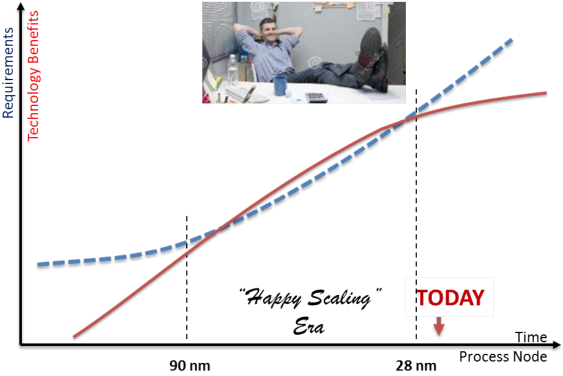


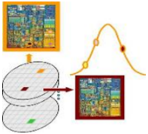

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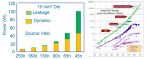


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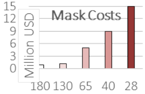


Skyrocketing NRE: mask & design cost.

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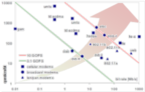

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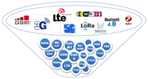

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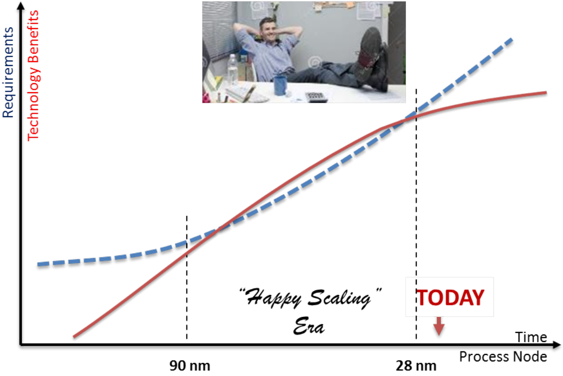


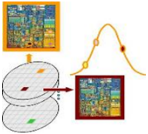

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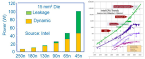

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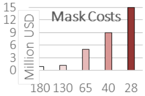


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## The Way Forward

1. Algorithm/hardware co-design is **more pertinent than ever**
2. Maintaining progress will require **cross-layer** and **interdisciplinary** innovation

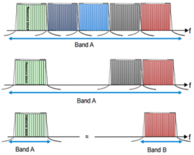
# Outline

1. **Classical algorithm/hardware co-design:**
   - Hardware implementation of successive cancellation list decoding of polar codes
   - Successive cancellation flip decoding of polar codes & its hardware implementation

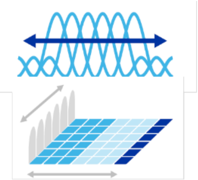
2. **Approximate computing:**
   - Throughput-oriented construction of polar codes
   - Error-correction coding on faulty hardware

3. **Communications hardware meets information theory and machine learning:**
   - Terabit/s LDPC code decoders via quantized message passing
   - Neural networks for self-interference cancellation in full-duplex radios

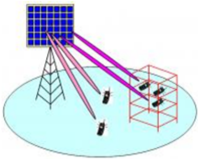
# Technology Innovations in 5G



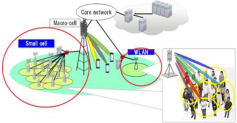

Wide Bandwidth and
Carrier Aggregation



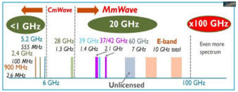
Flexible and Scalable
OFDMA Air-Interface



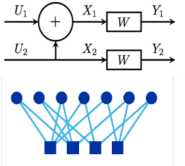
Massive MIMO




Small Cells and
Advanced Cellular Concepts




New Radio Frequencies
(mmWave)




**Advanced Channel Codes**
**(LDPC and polar)**

# Polar Codes

$\mathcal{A} = \{3, 5, 6, 7\}$

0
1
2
3
4
5
6
7

- Construction:
  - Information indices: $\mathcal{A} \subset \{0, 1, \ldots, N-1\}$, $|\mathcal{A}| = NR$, $N = 2^n$.

# Polar Codes

$$\mathbf{u} = \begin{bmatrix} u_0 \\ u_1 \\ u_2 \\ u_3 \\ u_4 \\ u_5 \\ u_6 \\ u_7 \end{bmatrix}$$

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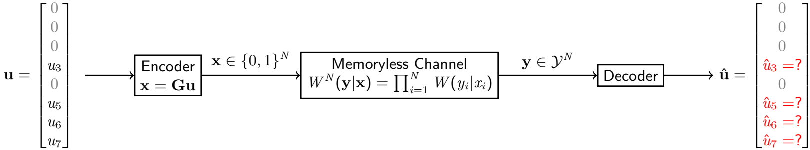


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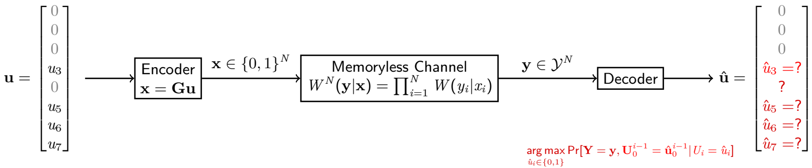


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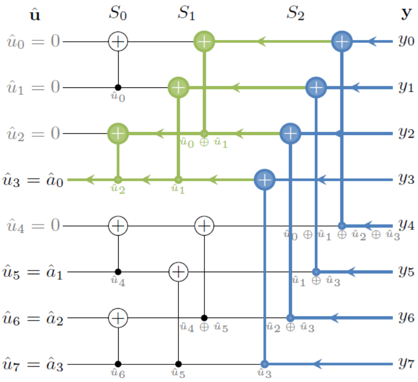
- Decoding: Estimate the information bits $\hat{\mathbf{u}}_{\mathcal{A}}$.
  - Successive Cancellation (SC) Decoding: At each level $i \in \mathcal{A}$, choose the best possible value of $u_i$ given the past estimations and frozen bits.

# Successive Cancellation Decoding

- Successive traversal of a data dependency graph
- $N \log N$ nodes, each visited exactly once $\longrightarrow$ $O(N \log N)$ **time complexity**!
- Re-use of memory positions $\longrightarrow$ $O(N)$ **memory complexity**!



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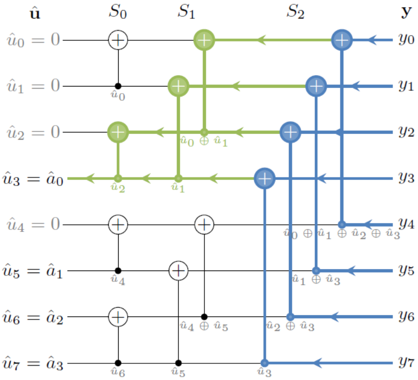
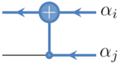
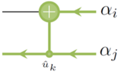



- Two simple soft information update operations:



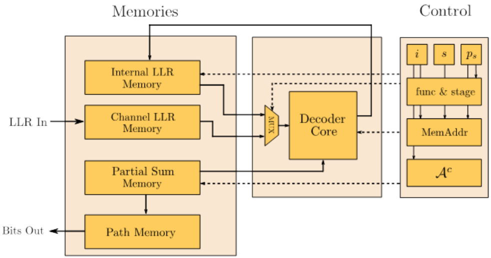

$$f(\alpha_i, \alpha_j) \approx \operatorname{sgn}(\alpha_i)\operatorname{sgn}(\alpha_j) \min\left(|\alpha_i|, |\alpha_j|\right)$$




$$g(\alpha_i, \alpha_j, \hat{u}_k) = \alpha_j + (-1)^{\hat{u}_k} \alpha_i$$

# Hardware Implementation of SC Decoding

- **Decoder Core:** contains $P$ processing elements that implement update rules
- **Memories:** store soft information, partial sums, and decoded codeword
- **Controller:** organizes memory reads and writes, and update rule selection



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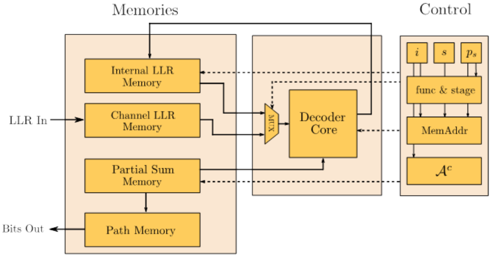


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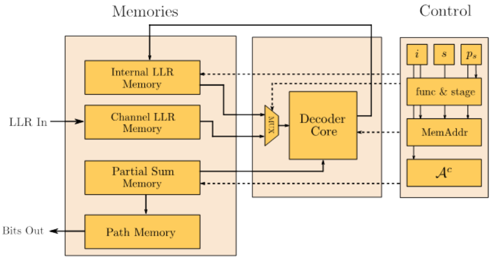


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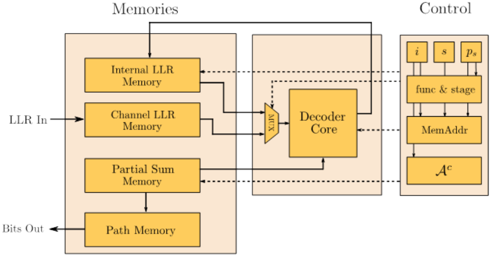


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  - **Time complexity:** $O(LN \log N)$, **Memory complexity:** $O(LN)$

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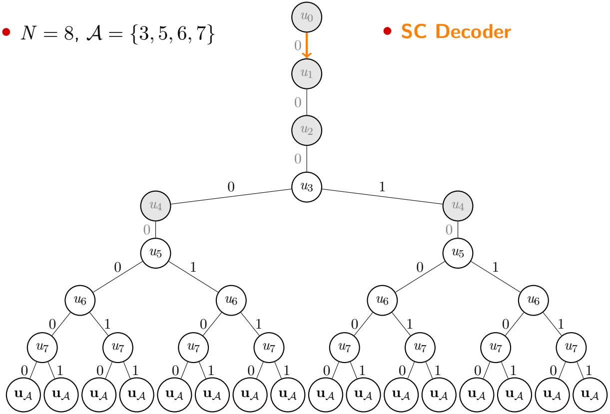


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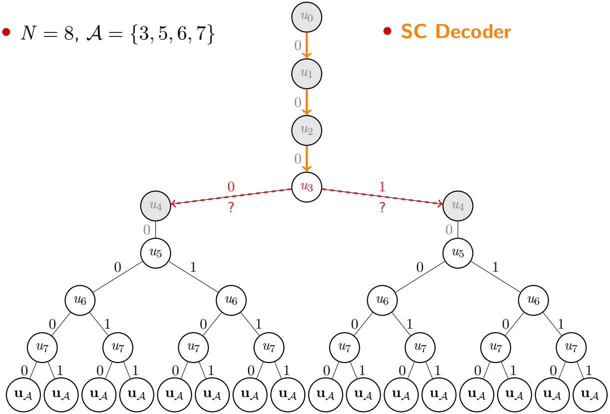


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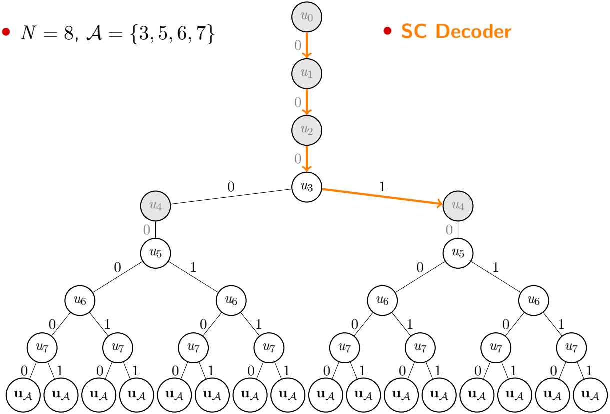


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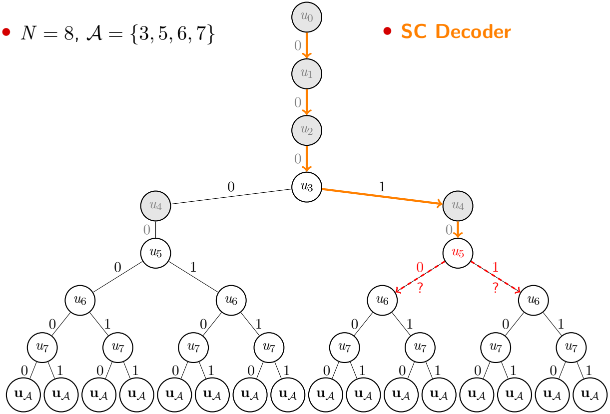


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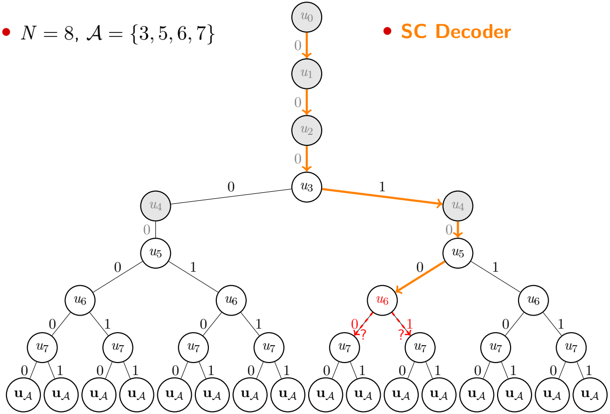


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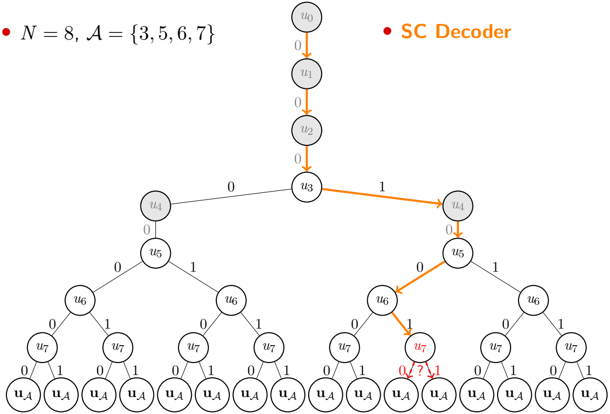

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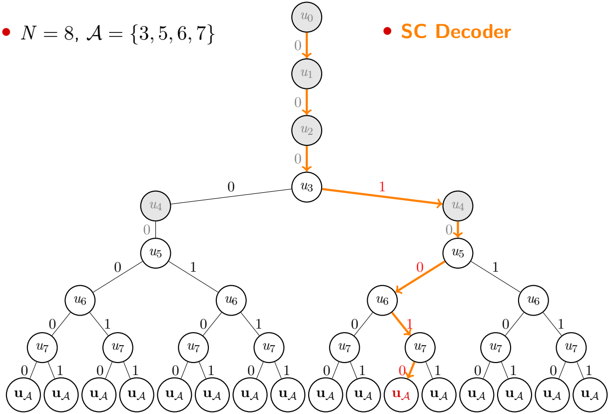

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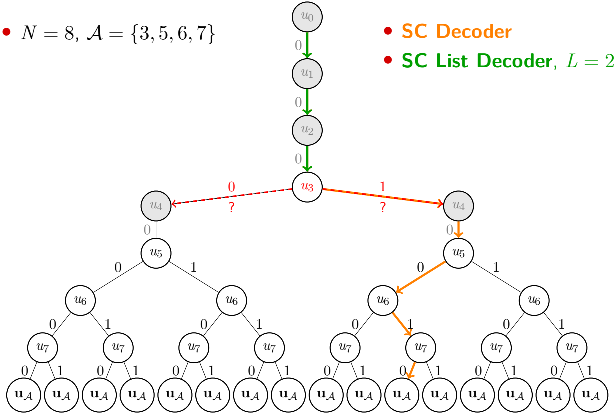


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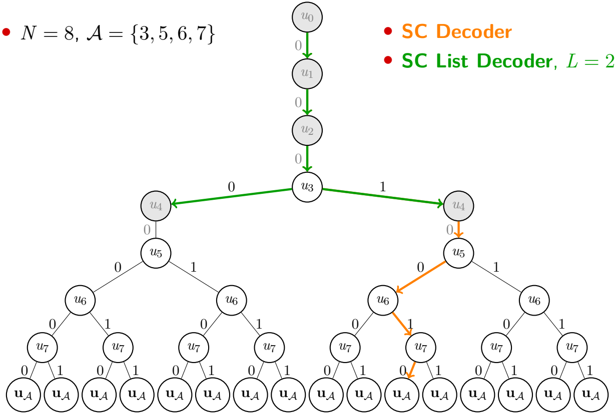


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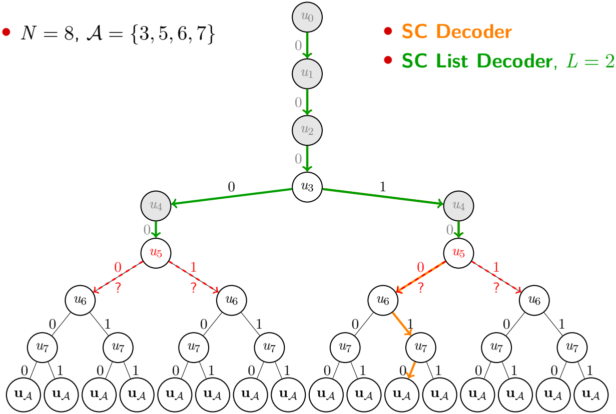


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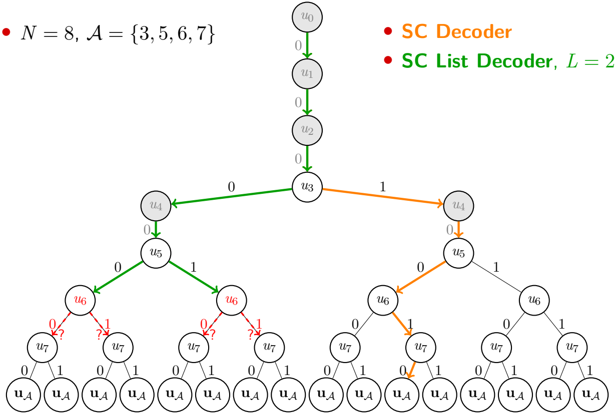


- **SC Decoder**
- **SC List Decoder**, $L = 2$

1 I. Tal, A. Vardy, "List decoding of polar codes," IEEE Transactions on Information Theory, May 2015

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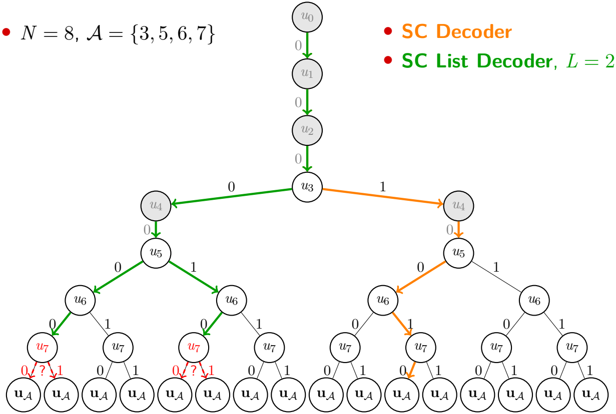


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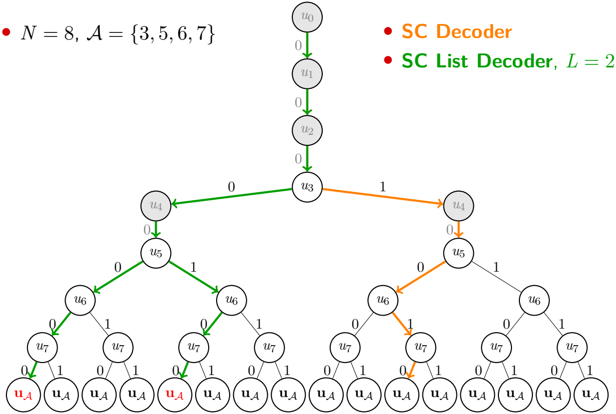

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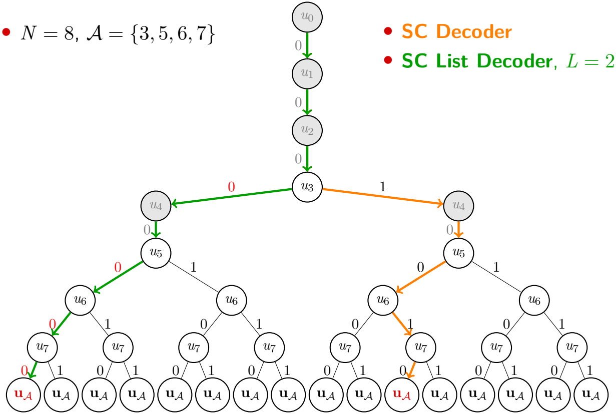


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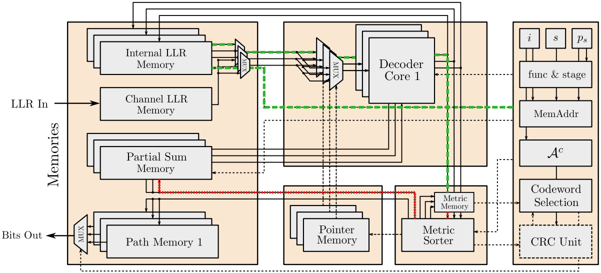
- Perform computations for $L$ paths simultaneously (highly parallelizable!)
- Compute and sort path metrics to keep $L$ best paths at each step

## What we need:

1. $L$ decoder cores
2. $L$ SC memories
3. A path metric sorter



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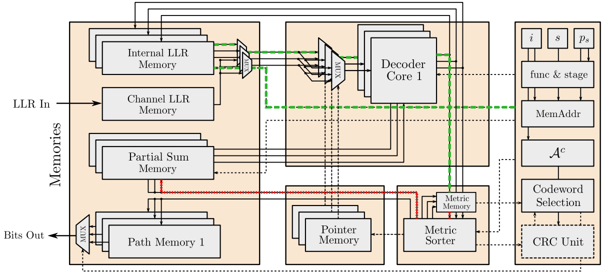


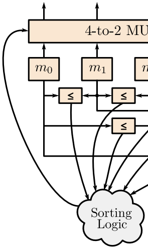

We proved an arithmetic re-formulation of SCL decoding that makes the hardware implementation **up to 67% more hardware-efficient**!

[1] A. Balatsoukas-Stimming, M. Bastani Parizi, A. Burg, "LLR-based successive cancellation list decoding of polar codes," IEEE Transactions on Signal Processing, Oct. 2015

# Optimized Metric Sorting for SCL Decoding

- Metric sorter lies on the **critical path** of SCL decoders

**Radix-$2L$ Sorter**

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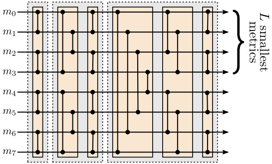


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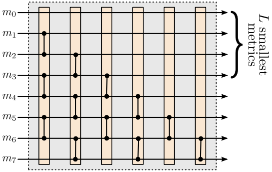

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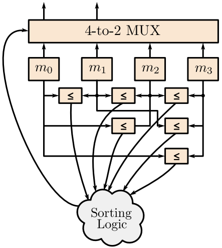


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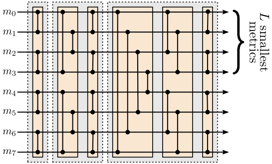


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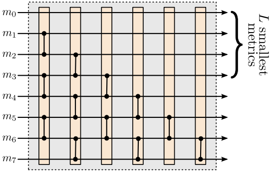

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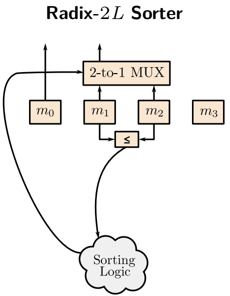


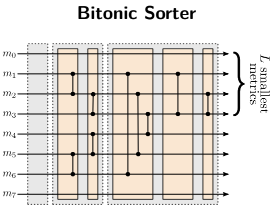


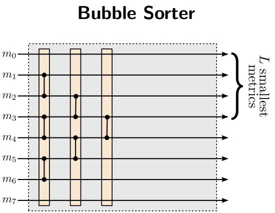


Significant improvement in the **area and operating frequency** of the decoder!

1. A. Balatsoukas-Stimming, M. Bastani Parizi, A. Burg, "On metric sorting for successive cancellation list decoding of polar codes," IEEE International Symposium on Circuits and Systems, May 2015

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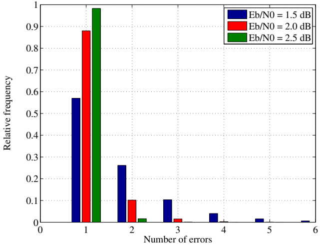

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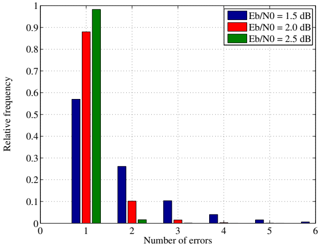


- **Successive Cancellation Flip** (SCF) decoding:
  1. Perform SC decoding and track $T$ most unreliable decisions
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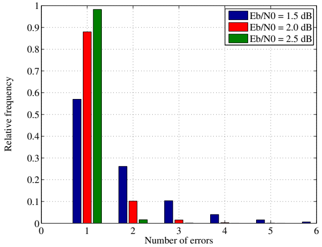


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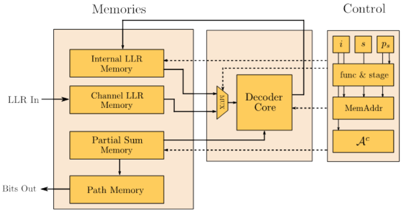
Error-correcting performance in-between SC and SCL, but:

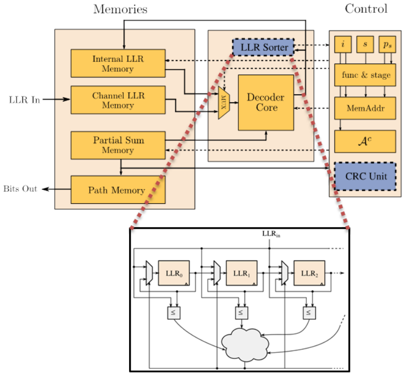
- **Memory complexity** of SC decoding
- (Average) **time complexity** of SC decoding (at high SNR)

1 O. Afisiadis, A. Balatsoukas-Stimming, and A. Burg, "A low-complexity improved successive cancellation decoder for polar codes," in Asilomar Conf. on Signals, Systems, and Computers, Nov. 2014

# Hardware Implementation of SCF Decoding

- **Simple:** Add an insertion sorter and a CRC unit to an SC decoder

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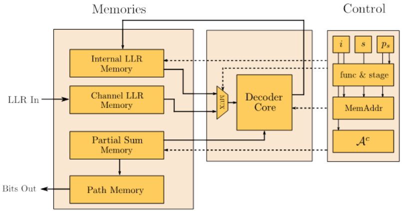


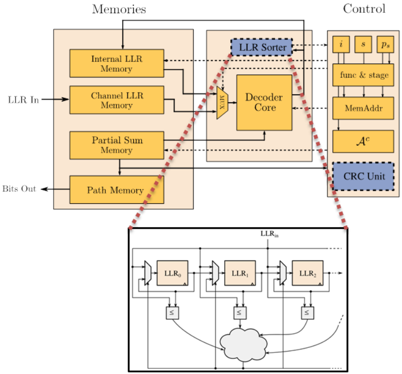


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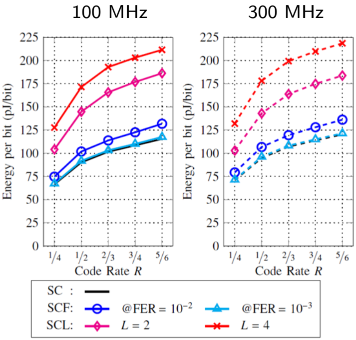
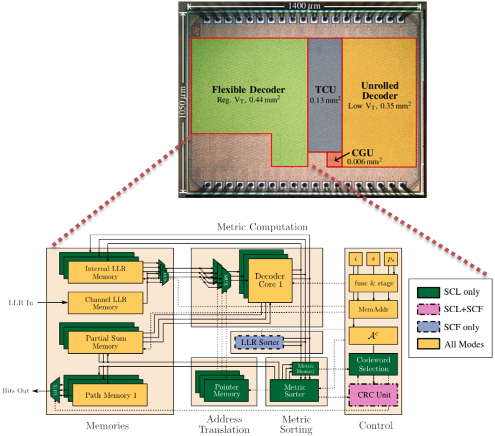
**Our proposed SCF decoding algorithm** is being considered by the 3GPP as an ultra-low power option for massive machine type communications for IoT in 5G

1 Huawei and HiSilicon, "Computational and implementation complexity of channel coding schemes," 3GPP TSG RAN WG1 Meeting #86, Tech. Rep. R1-167213, Aug. 2016

# Bringing It All Together

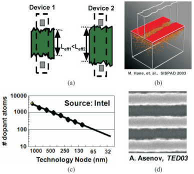
- PolarBear: Manufactured ASIC in **ST 28 nm FD-SOI**
  - SC, SCF, and SCL decoding on the same chip
  - Run-time algorithm selection for **energy-proportional operation**



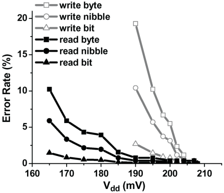




1 P. Giard, A. Balatsoukas-Stimming, C. Müller, A. Bonetti, C. Thibeault, W. J. Gross, P. Flatresse, A. Burg, "PolarBear: A 28-nm FD-SOI ASIC for decoding of polar codes," IEEE Journal on Emerging and Selected Topics in Circuits and Systems, Dec. 2017

# VLSI Circuits are Becoming Unreliable




Process variation
[K. Roy et al., 2010]

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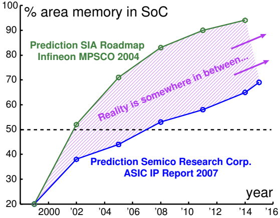


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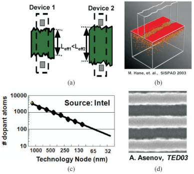


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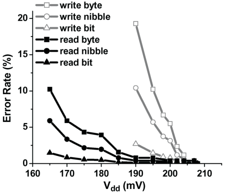


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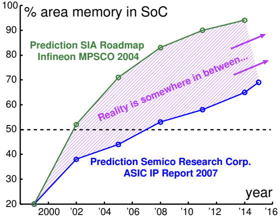


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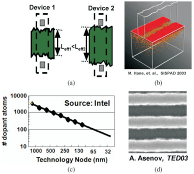


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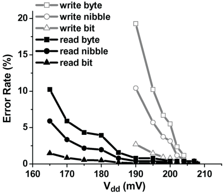


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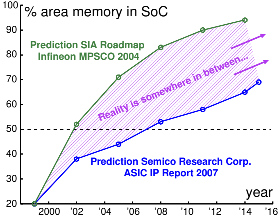


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## What to do?

- Hardware protection to avoid errors is costly in terms of area and power
- Discarding faulty chips can decrease the yield dramatically

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- Throughput-oriented construction of polar codes
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- Faulty min-sum decoding of LDPC codes
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1. A. Balatsoukas-Stimming, G. Karakonstantis, A. Burg, "Enabling complexity-performance trade-offs for successive cancellation decoding of polar codes," International Symposium on Information Theory (ISIT), Jun. 2014
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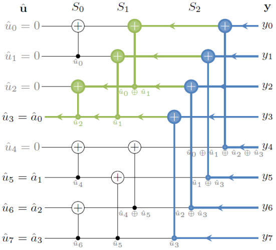
# Throughput-Oriented Construction of Polar Codes

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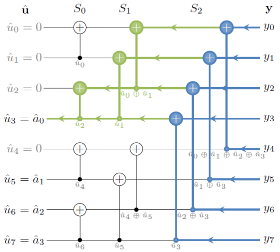


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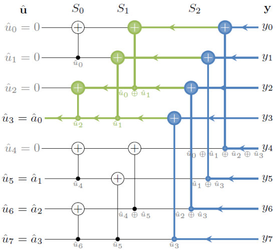


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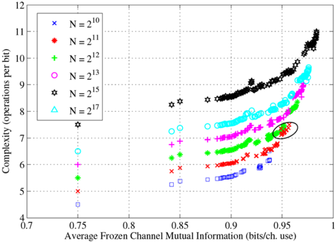
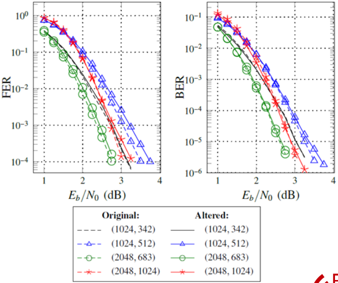
**Numerous complexity-performance trade-offs**




**Minimal performance degradation**



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- Binary Erasure Channel (BEC):
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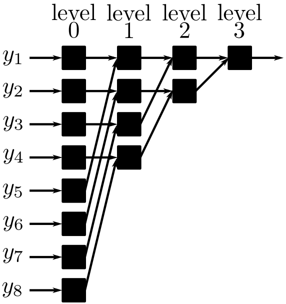


## Density Evolution

- Erasure probability at $f$ **nodes**: $T^f(\epsilon) = 2\epsilon - \epsilon^2$
- Erasure probability at $g$ **nodes**: $T^g(\epsilon) = \epsilon^2$

# Density evolution for faulty SC decoding

- We describe failures in a memory cell as unreliable computations

**Fault model**

Additional erasures appear in **non-erased** outputs with probability $0 < \delta < 1$

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## Theorem (**All channels** become asymptotically **useless**)

*Under faulty SC decoding over the BEC,* $\epsilon_j \xrightarrow{\text{a.s.}} 1$.

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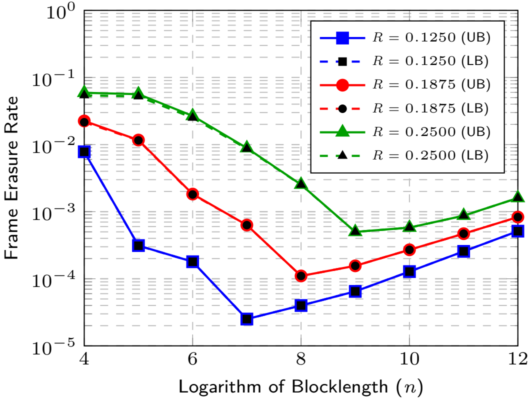

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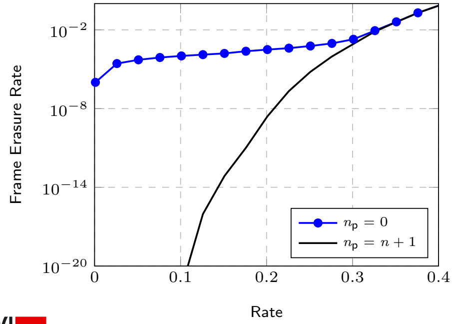


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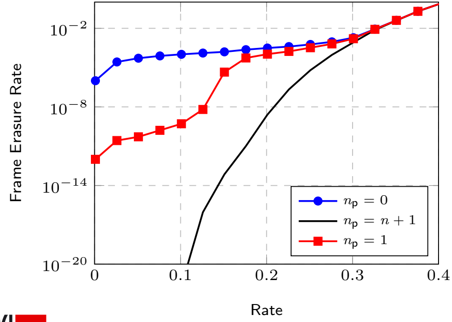


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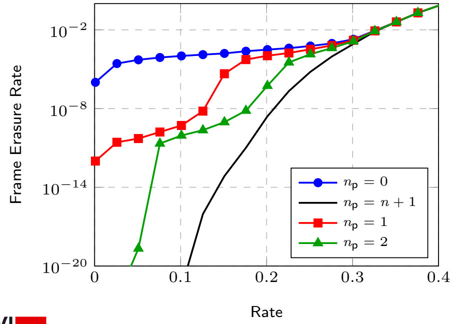


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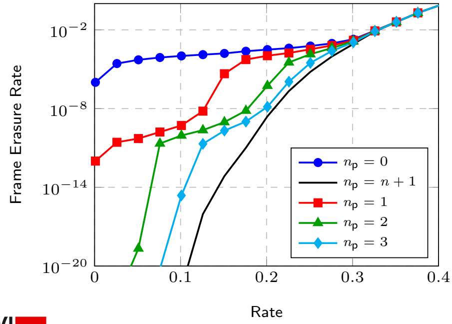


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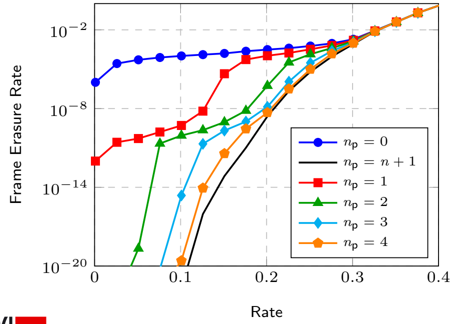


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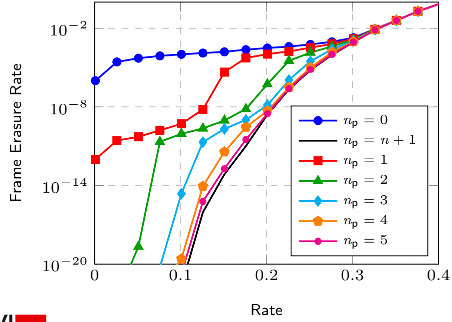


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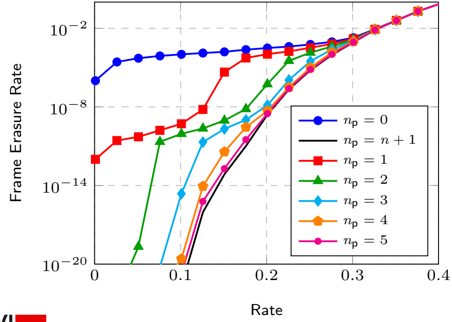


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# Outline

1. **Classical algorithm/hardware co-design:**
   - Hardware implementation of successive cancellation list decoding of polar codes
   - Successive cancellation flip decoding of polar codes & its hardware implementation

2. **Approximate computing:**
   - Throughput-oriented construction of polar codes
   - Error-correction coding on faulty hardware

3. **Communications hardware meets information theory and machine learning:**
   - Terabit/s LDPC hardware decoders via quantized message passing
   - Neural networks for self-interference cancellation in full-duplex radios

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- An LDPC code can be represented as a Tanner graph with:
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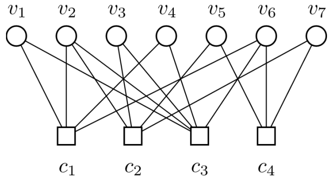
  - **Check nodes** (CNs)




## Min-Sum Decoding

$$\text{Variable-to-check messages:} \quad \Phi_v(L, \boldsymbol{\mu}) = L + \sum_i \mu_i,$$

$$\text{Check-to-variable messages:} \quad \Phi_c(\boldsymbol{\mu}) = \prod_j \operatorname{sign} \mu_j \, \min |\boldsymbol{\mu}|.$$

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## Finite-Alphabet Message-Passing

Quantization $\longrightarrow$ Decoding Algorithm

- Updates are implemented as optimized look-up tables (LUTs).
- Potential for **significant bit-width reduction and performance improvement**.

1. R. Ghanaatian, A. Balatsoukas-Stimming, C. Müller, M. Meidlinger, G. Matz, A. Teman, and A. Burg, "A 588 Gbps LDPC decoder based on finite-alphabet message passing," IEEE Transactions on Very Large Scale Integration Systems, Feb. 2018
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3. A. Balatsoukas-Stimming, M. Meidlinger, R. Ghanaatian, G. Matz, and A. Burg, "A fully-unrolled LDPC decoder based on quantized message passing," in IEEE International Workshop on Signal Processing Systems (SiPS), Oct. 2015

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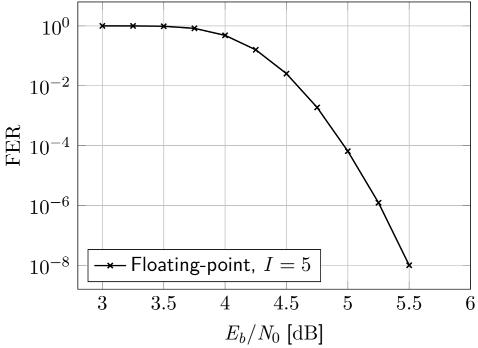

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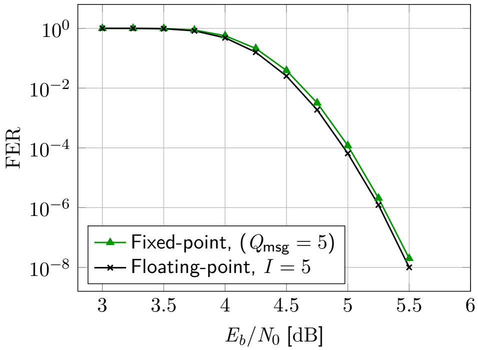

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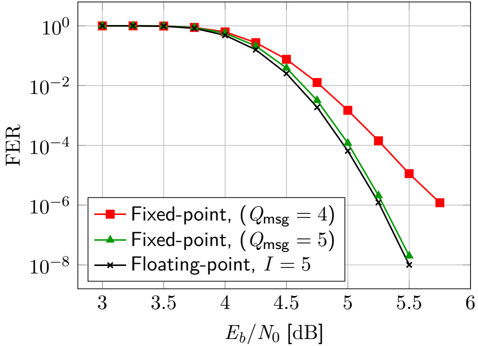

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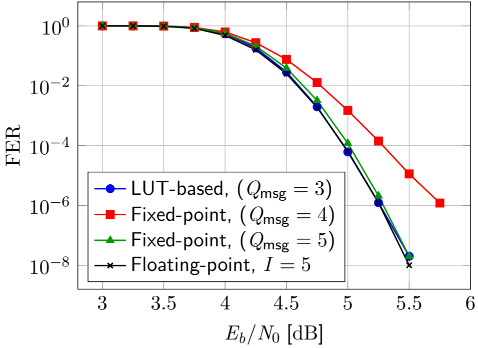

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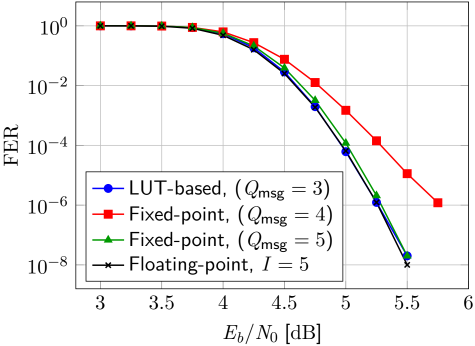
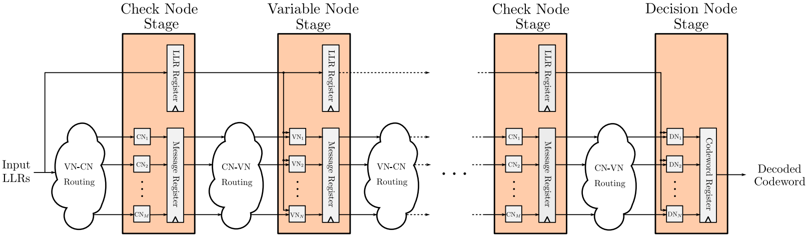



**40% message bit-width reduction** with identical FER performance.

# Fully Unrolled LDPC Decoder Hardware Architecture

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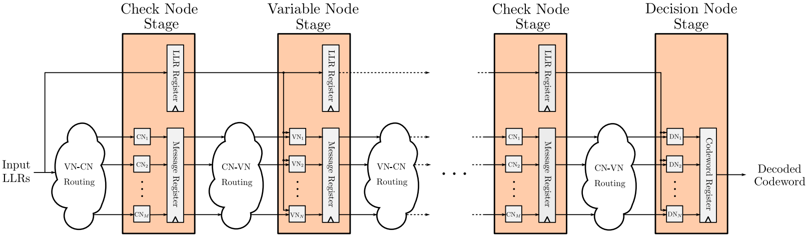


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| | Quant. MS | LUT-based | |
|---|---|---|---|
| Area ($\text{mm}^2$) | 35.63 | 33.79 | **−5%** |
| Throughput (Gbps) | 1014 | 1665 | **+64%** |
| Area Eff. ($\text{Gbps}/\text{mm}^2$) | 28.46 | 49.27 | **+73%** |

# Bi-directional Wireless Communications

## Time-division duplexing (TDD)

Wasted time resources: switching interval


## Frequency-division duplexing (FDD)

Wasted frequency resources: guard bands


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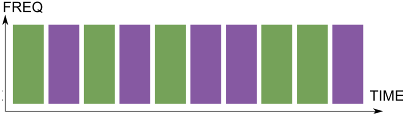


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**Fundamental Challenge:** Self-interference is much stronger than the desired signal!

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**Example**

For $P = 7$ and $M + L = 13$ memory taps $\rightarrow$ $20$ basis functions and $260$ parameters!

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## Idea

Why not use a **neural network** that **extracts structure** from training data?

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2 A. Balatsoukas-Stimming, "Non-linear digital self-interference cancellation for in-band full-duplex radios using neural networks," IEEE International Workshop on Signal Processing Advances in Wireless Communications (SPAWC), Jun. 2018 (accepted)

# Self-Interference Cancellation Using Neural Networks

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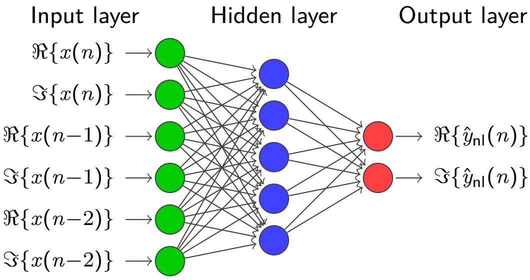

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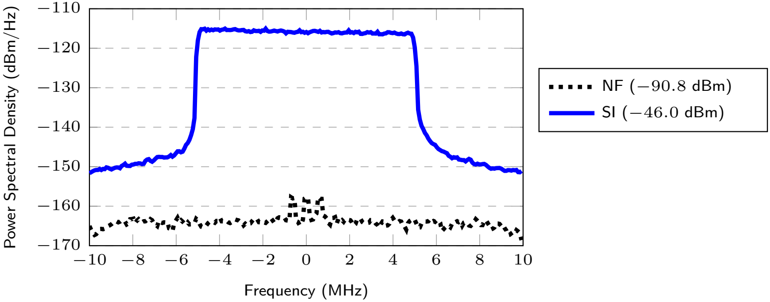

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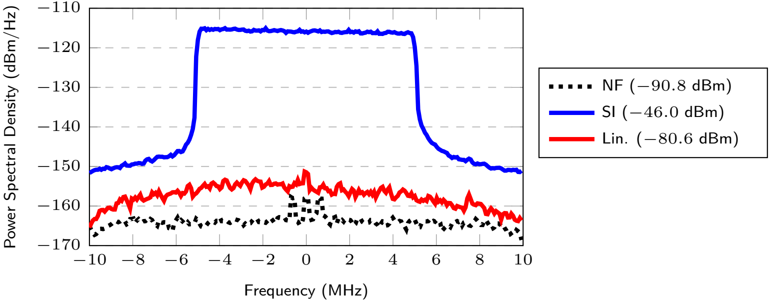

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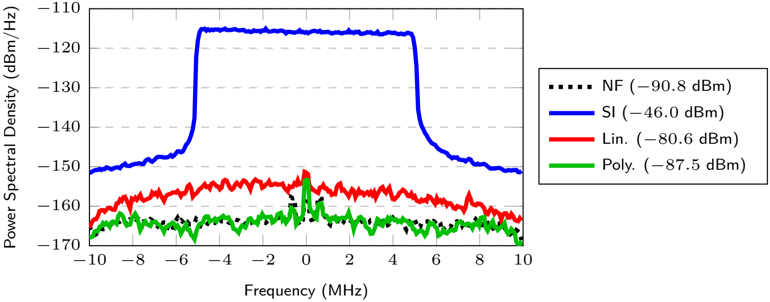
- 10 MHz OFDM signal, 56 dB passive cancellation, $M + L = 13$ taps



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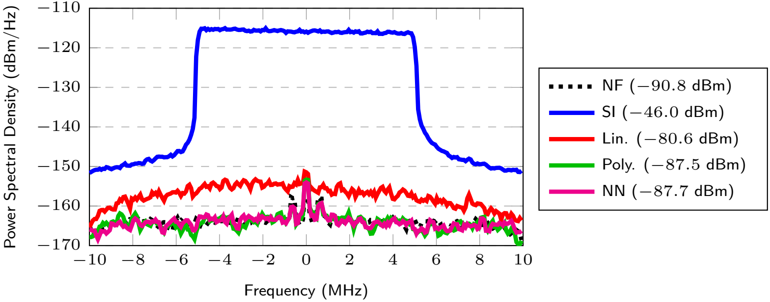

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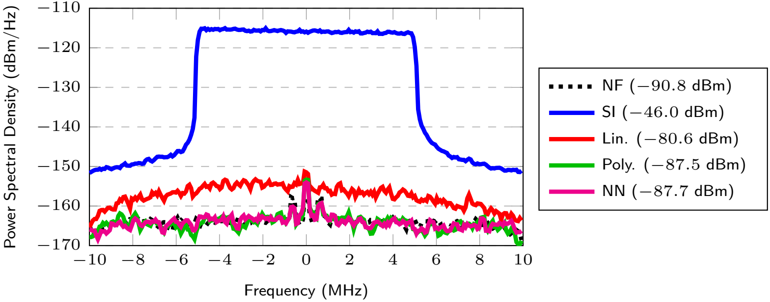


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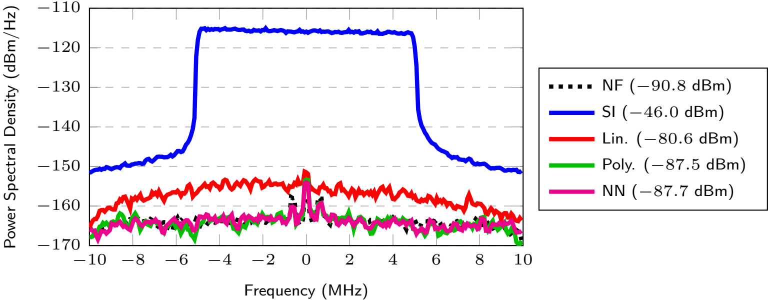


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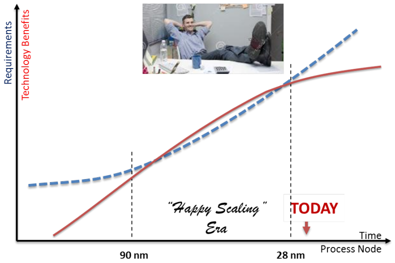
**Identical** cancellation performance with **lower complexity**!

# Conclusions




- A combination of approaches is necessary to maintain progress in the **post-happy-scaling era**, including:
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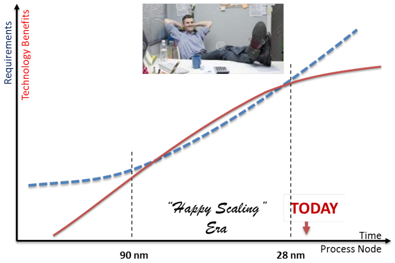


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The end of the happy scaling era creates new **challenges and opportunities** for innovation!